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# DESIGN OF BALANCED DIFFERENTIAL PAIR BASED CCCII CIRCUIT AND CONFIGURABLE FREQUENCY AGILE FILTER APPLICATION IN 28nm PROCESS

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***Abstract –*** *Connectivity in any terms between machine to machine, machine to people or vice versa and between people is getting more importance in todays` community life. This reality leads to an increasing interest for intensified and complex communication standards to be used or investigated. One of the most important candidate solutions for these kinds of communications are encrypted and cognitive communication techniques. Main characteristic advantages of the circuits used in encrypted and cognitive communication systems will be highlighted as, agility and configurability. In this study, it`s aimed to provide circuit solutions for encrypted and cognitive communication systems with lower power consumption and higher bandwidth with respect to the investigated ones in the literature. CCCII circuits in this study are designed with STMicroelectronics` 28nm Process to take advantageous properties of a top notch process and applications with frequency agile and configurable filters realized as a first example application in this process. Main goal of this study is to support different GPS protocols with unique filter circuit as an application.*
***Keywords -*** *Balanced differential pair, CCCII, Frequency Agile, Configurable, Filter.*

## 1. Introduction

In the last decades, societies` needs and interests on communication and information sectors increased crucially and staying to be connected to any kind of data or information gained more importance than it was before. Furthermore, technological developments revealed in these environments constituted the key issues not only in economical spectrum but also in cognitive environments. The emergence of searching or implementing new standards to support this complex environment is a direct result of the increased usage in both number and types of voice, data and complex content transmissions at great speeds beyond the limits, [1 – 7]. Standard specific, private communication circuit implementations during the improvement period of such systems have led to great complexity and number of components in later steps. Implemented or designed structures suffer from supporting only single determined standard or application, [1 – 5]. In the past years, the focus moved to provide configurable, common circuit structures to support multiple communication standards. To overcome the difficulties of providing solution to such environments, circuits with fast frequency response, wider bandwidths, lower power consumption and configurability are getting higher importance day by day.

The advantages brought by the technological improvements and powerful features of current-mode circuits when compared to voltage-mode circuits such as, high operating frequencies and low power consumption have changed the approach to current-mode circuits and these kind of circuits gained importance due to the listed properties. An analog three port component, second generation current conveyor (CCII), has gained importance in designs due to the provision of high-bandwidth, wide dynamic operating ranges and high slew rate (SR) values in addition to its` voltage mode equivalents, [8]. Later on, the introduction of the second generation current controlled current conveyor (CCCII) responded the main drawback in lacking of electronically tunable feature of CCII by utilizing the parasitic floating intrinsic terminal resistance at port X, [9].

In both literature and industrial applications, there are various types of CCCII structures investigated and implemented. Each of these structures differ from any other in terms of number of elements, power consumption, bandwidth and dynamic operating ranges. In this study, due to the low supply voltage limitations

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of the process, a fully CMOS balanced differential pair based CCCII structure implemented. The CCCII structure designed and all important characteristics are observed with the aid of well designed simulation environments. Considering its possible industrial applications to support multiple Global positioning systems (GPS), a frequency agile, configurable filter is designed and its behaviors analyzed by the simulations. This study is an extended and improved version of a previous work, [2].

## 2. Design of CCCII

Characteristic representation of an inverting or non-inverting type of CCCII structure will be given with mathematical expressions by the following matrices, [9]:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (1)$$

The current output at port Z($i_z$) that is conveyed from the input current at port X($i_x$) is expressed as, [9]:

$$i_z = \pm i_x = \pm (v_x - v_y)/R_x \quad (2)$$

As it can be easily derived from the formulas, the CCCII based applications can be realized resistor-free and tunable by utilizing terminal resistance $R_x$ as the adjustable circuit's parameters.

The ideal equivalent circuit of CCCII is displayed in Figure 1 for better understanding, [9].

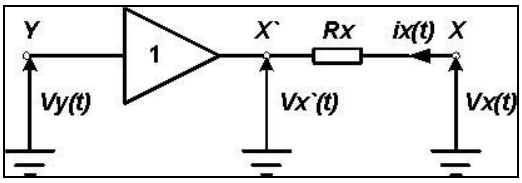


**Figure 1.** Equivalent circuit of CCII structure, [9].

### 2.1. Balanced Differential Pair Based CCCII Structure

During the initial feasibility phase of the design, different circuit topologies are investigated in details. In the implementation phase, it is seen that the supply voltages (±0.5V) of 28nm process will limit the maximum number of elements to be placed rail-to-rail.

Since commonly used architectures do not provide any solution for the low voltage operation at this process node, it is decided to implement balanced differential pair based CCCII structure with its additional built-in advantages, [10].

Circuit representation of the designed structure is given in Figure 2.

The current-relationship between port X and Z of the balanced differential-pair CCCII can be expressed as, [10]:

$$i_x = i_{p2} + i_{n4} \cong i_{p4} + i_{n3} \cong i_z \quad (3)$$

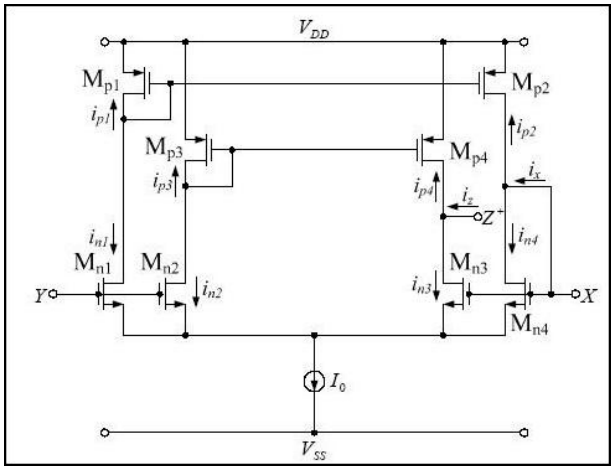


**Figure 2.** Balanced differential-pair based CMOS CCCII, [10].

The output resistance of any Z-port of the balanced differential-pair CCCII is simply characterized based on the attached MOSFETs as, [10]:

$$r_o = 1/(g_{ds}^{PMOS} + g_{ds}^{NMOS}) \quad (4)$$

The terminal resistance ($r_x$) is still dependent on the transconductance of NMOS differential-pair ($g_{md}$), which can be expressed as, [10,11]:

$$R_x = (v_x - v_y)/i_x \cong 1/g_{md} \cong 1/\sqrt{\mu_n C_{ox} \frac{W_n}{L_n} I_o} \quad (5)$$

Lastly, in the balanced differential-pair structure, as $V_x >> V_y$, $M_{n1}$ and $M_{n2}$ are virtually off, while nearly conduct whole bias-current when $V_x << V_y$. Therefore $I_X^{max}$ and $I_X^{min}$ can be approximated to following equation, [10]:

$$|V_{XY}| \le \sqrt{I_o/(\mu_n C_{ox} \frac{W}{L})} \quad (6)$$

## 2.2. Designed Differential Pair Based CCCII Structure

The realization of the balanced differential pair CCCII structure is done according to the version proposed in the literature [9], with two non-inverting Z ports to provide design flexibility in frequency agile filter realization, which is shown in Figure 3. It is also possible to add inverted outputs or more non-inverting output ports under some constraints, [10].

STMicroelectronics 28nm bulk CMOS process used for the design of the circuit with ±0.5V supply voltages and simulations held with the aid of Spectre environment. Minimum length of the transistors used in the design is selected as 120nm, which is 4 times of the minimum allowed value 30nm, to increase finite output resistance values.

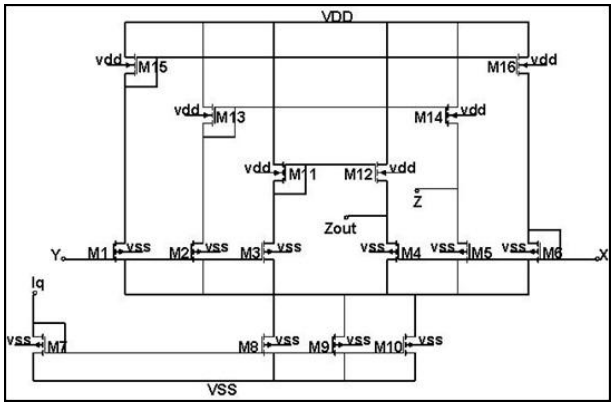


**Figure 3.** Designed balanced differential-pair CCCII structure with two Z ports.

Aspect ratios(W/L) of the MOSFETs will be listed as; $M_1 – M_6$: 20, $M_7 – M_{10}$: 30, $M_{11} – M_{16}$: 50.

## 2.3. Simulation Results of the Designed CCCII Circuit

The characteristic of Rx relating to 10µA bias-current is presented in Figure 4. Its frequency-dependence can be easily approximated by a model having one real zero and a pair of complex poles.
Observing Figure 4, the resistance value seen on port x remains flat up to 1.45GHz frequency values, which is very efficient for our application range.

The large signal characteristics are simulated again at 10µA bias-current to prove the compatibility of the used balanced differential pair based structure and the CCCII theorem.

In Figure 5, the voltage transfer characteristics are plotted, which is showing the exact voltage following performance of Y and X. Additionally, the V-I characteristic of the input voltage versus the input current at port X is revealed in the same figure. This behavior verifies the approximated balanced dynamic range and very low offset voltage.

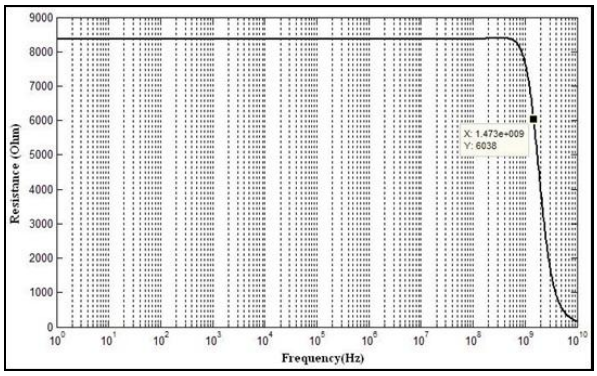


**Figure 4.** $R_x$ based on $I_0$=10µA.

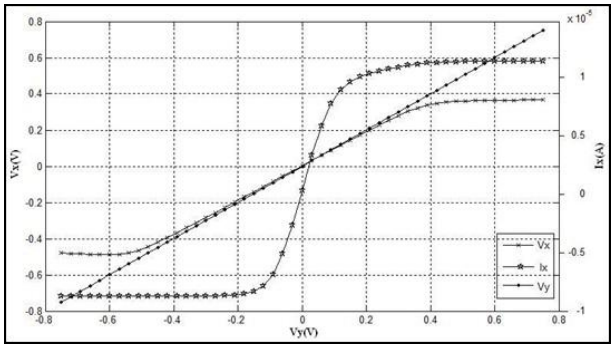


**Figure 5.** The voltage transfer and voltage-current characteristics of CCCII.

The small-signal current transfer gain characteristic of the designed CCCII circuit is plotted in Figure 6 and the transient current follow between port Z and X is shown in Figure 7 for 500MHz signal input.

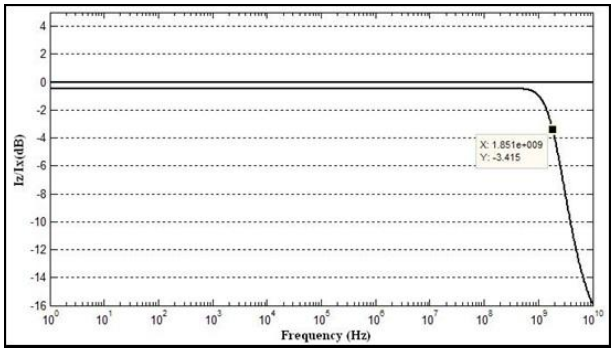


**Figure 6.** The small-signal characteristic of the current transfer gain.

At corresponding bias current, the frequency characteristics of the designed circuit in operation can

be assumed to be dominated by terminal resistance bandwidth. This can be also referred as open loop bandwidth of the circuit.

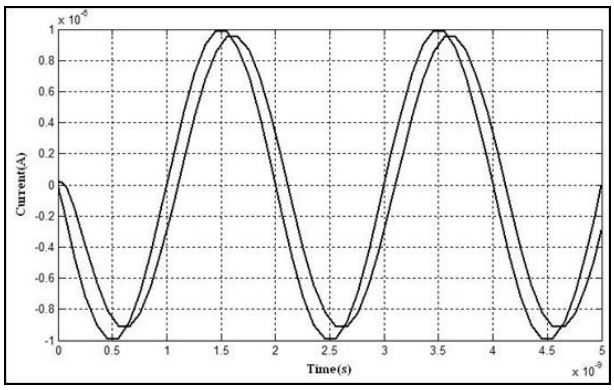


**Figure 7.** Transient current transfer characteristic between ports X and Z.

All in all, after observing main large and small signal behaviors of the designed CCCII circuit, it is very clear that it is suitable for high frequency applications with the advantages of high end process node of 28nm.

## 2.4. Corner Simulations of the Designed CCCII Circuit

Corner simulations for the designed CCCII circuit are also executed to see circuit behavior under industrial standards. To do this, in addition the default process variables scattering, temperature max-min variables defined as -40˚C and 110˚C, bias current scattering factor is defined as %25, which leads to 7.5µA and 12.5µA for a 10µA bias current and finally supply voltage scattering factor is defined as %10, which leads to ±0.45V and ±0.55V for a ±0.5V supply voltage.

In order to verify the balanced differential pair based CCCII architecture that is investigated in previous sections, 72 different corners are obtained over defined temperature, process parameters, supply voltages and bias currents.

The characteristic of $R_x$ relating to corner analysis results are presented in the figure 8. From the given figure, maximum value observed for the resistance is 13.14kΩ that remains flat up to 2.10GHz for 7.5µA bias current, ±0.45V supply voltage, 110˚C temperature. Minimum resistance value obtained is, 5.35kΩ that remains flat up to 5.10GHz for 12.5µA bias current, ±0.55V supply voltage, -40˚C temperature.

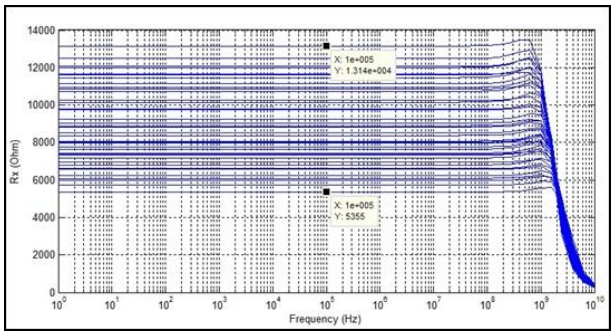


**Figure 8.** $R_x$ based on 72 different corners.

In Figure 9, the voltage transfer characteristics are plotted for various corners, which shows the exact voltage following performance of Y and X ports for corners. This figure verifies the approximated balanced dynamic range and very low offset voltage for different conditions.

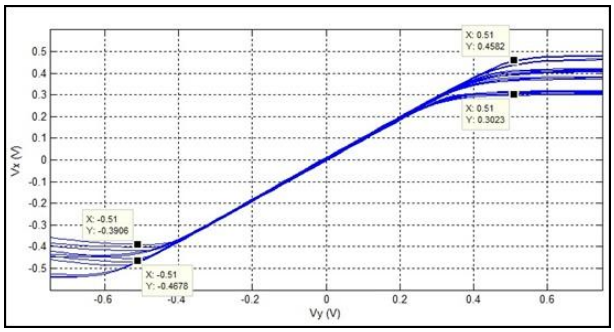


**Figure 9.** The voltage transfer characteristics of CCCII for corner analysis.

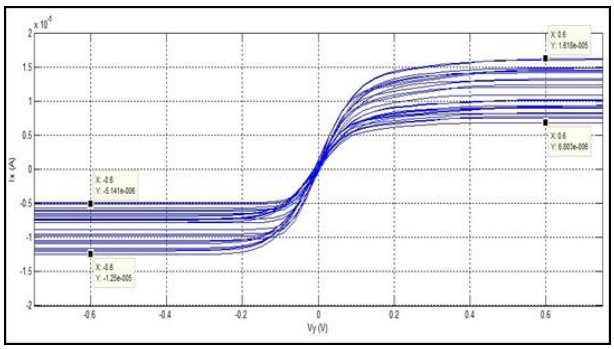


**Figure 10.** The voltage-current($V_y$ - $I_x$) characteristics of CCCII for corner analysis.

The characteristic of the input voltage versus the input current at port X is revealed in Figure 10. Maximum offset current flowing through port x is observed as 1.8µA for operating conditions at 12.5µA bias current, ±0.55V supply voltage, 110˚C temperature. Minimum offset current flowing through port x is observed as

24nA for operating conditions at 12.5µA bias current, ±0.45V supply voltage, -40˚C temperature.

The small-signal current transfer gain characteristic of the designed CCCII circuit is plotted in Figure 11 for the mentioned corner cases. Maximum value observed for current transfer ratio is -368mdB for 7.5µA bias current, ±0.55V supply voltage, -40˚C temperature and minimum value observed for current transfer ratio is -668mdB for 7.5µA bias current, ±0.45V supply voltage, 110˚C temperature.

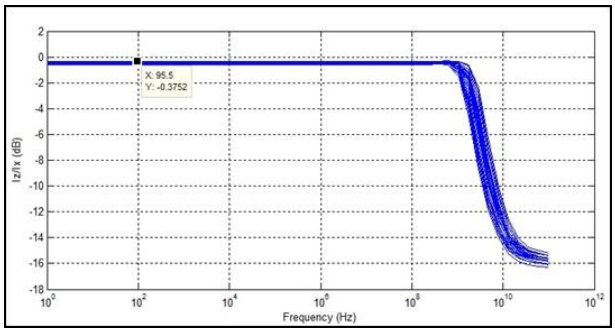


**Figure 11.** The frequency current gain ($I_z/I_x$) characteristics of CCCII for corner analysis.

Additionally, the 3-dB bandwidth of current gain for different cases can be approximately read from Figure 11 as maximum 3.75GHz for 12.5µA bias current, ±0.55V supply voltage, -40˚C temperature and it is read as minimum 1.51GHz for 7.5µA bias current, ±0.45V supply voltage, 110˚C temperature.

## 3. Layout and Post-Layout Simulations

The last and the foremost part for any design activity is the layout drawing of the design in industrial design cycle. In this project, since the used process is an industrially available design kit library, it is planned to implement layout drawing and post-layout simulations of the designed circuit. During these steps, layout of the designed circuit is drawn with Layout XL tool. For the sake of the flow, design rule checking run on the layout with Calibre DRC tool with full recommended rule sets. As the next step of the flow, layout versus schematic (LVS) comparison ran with Calibre to cross check the existance of problems or mismatches between the schematic design and layout. Extraction, as the last step of layout flow, is executed with Calibre PEX, PVE with full resistor and capacitance extraction in line with the provided rule sets.

During the entire flow, as the provider of the process design kit, STMicroelectronics` recommended rule sets checked carefully.

### 3.1. Layout Drawing

The transistors used in this design are bulk CMOS process transistors with low threshold properties. Although various types of transistors are provided with the design kit, used components are the bottom limit for allowed components to be implemented.

Layout of the balanced differential pair based CCCII structure is drawn with respect to all mentioned items in layout procedures.

Layout drawings of the balanced differential pair based CCCII circuit are given with Figures 12 and 13.

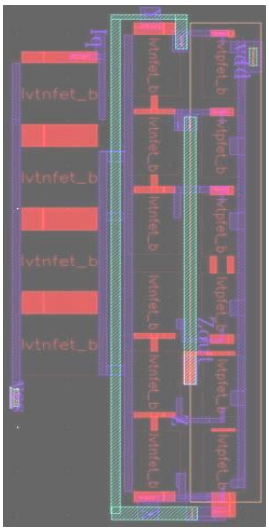

**Figure 12.** Layout of the balanced differential pair based CCCII(1).

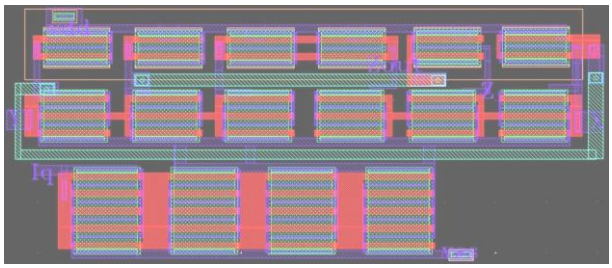

**Figure 13.** Layout of the balanced differential pair based CCCII(2).

### 3.2. Post-Layout Simulations

Following the layout extraction of the CCCII circuit, execution of post-layout simulations realized to test behavior of the latest structure with respect to schematic simulations.

Characteristics of the extracted CCCII circuit for the same supply values and bias currents are given with the Figures from 14 to 16.

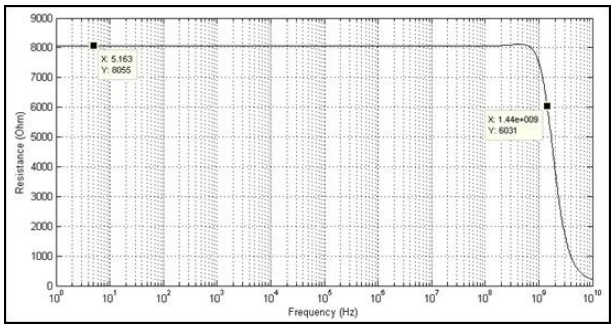


**Figure 14.** $R_x$ vs frequency.

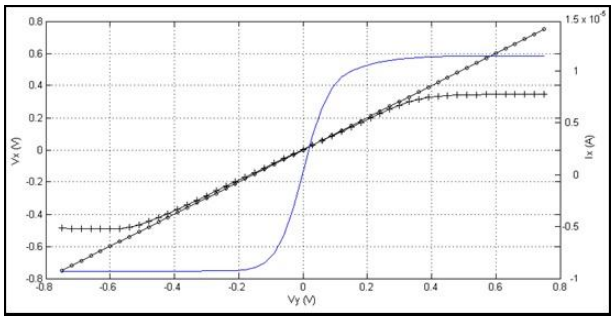


**Figure 15.** The voltage transfer and voltage-current characteristics of CCCII.

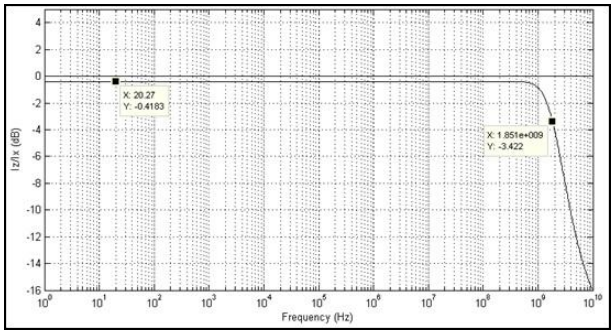


**Figure 16.** The small-signal characteristic of the current transfer gain.

After observing all characteristics same as the pre-layout version of the simulations, although there are some performance degredations exist after extraction of layout, they are not crucial to the operation of the designed CCCII. So, it is very clear that the extracted version is suitable for the application in high frequency ranges.

## 4. Filter Application

In order to facilitate the advantages of the process technology and configuration of the CCCII structure, a novel frequency agile fully active filter structure, which is proposed by Fabre and his team, is chosen for the application. In these types of communications, to adress the needs of environments, cognitive, sensing and self arranging structures are mainly needed for the implementation and to increase efficiency in the communication environment.

The implementation of the frequency agile filter is based on the proposed structure by Fabre and the team, [12]. The structure is mainly based on a classical second order filter structure with two different outputs at least: band-pass and low-pass [12]. Figure 17 shows the classical voltage mode second order filter circuit with two outputs. This cell is called as class 0 filter which is the basic element for the implementation of a frequency agile filter, [12].

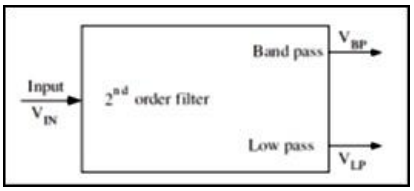


**Figure 17.** Basic second order filter including two different outputs, [12].

The input voltage of the filter is $V_{in}$, its band pass and low pass outputs are $V_{BP}$ and $V_{LP}$. Transfer functions for the two outputs are, [12]:

$$F_{BP}(s) = (V_{BP}/V_{IN})(s) = (a's)/(1+as+bs^2) \quad (7)$$

$$F_{LP}(s) = (V_{LP}/V_{IN})(s) = d'/1+as+bs^2 \quad (8)$$

Figure 18 shows the new second order frequency agile filter circuit obtained from the basic cell given by Figure 17. It is called by the team as class 1 frequency agile filter, [12].

Table 1 summarizes the characteristics of the agile filter derived from the structures shown in Figure 17 and 18.

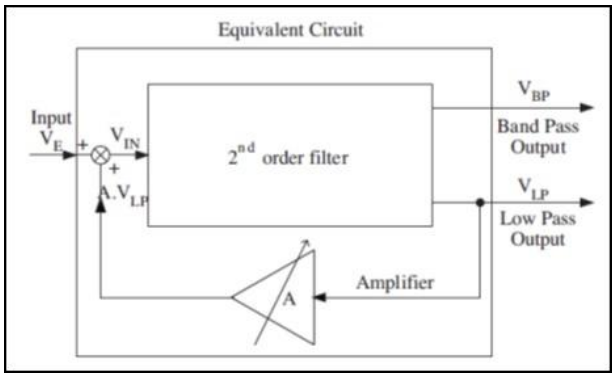


**Figure 18.** Frequency agile filter made from the basic cell, [12].

### 4.1. Frequency Agile, Configurable Filter Application

The CCCII circuit is considered to be used in a cognitive and encrypted communication standard like multi protocol GPS environment application due to the cognitive structure`s proximity investigated and proposed by Fabre and the team. In recent implemented system on chip (SoC) structures, discrete or dedicated filter stages are implemented to support continental specific positioning protocols. In this work, implemented filter structure provides multi-protocol positioning system handling without any need for additional circuitry and this shows it will replace the place of present discrete solutions effectively. Signals will be easily extracted from their carries frequencies with the aid of mixers and center frequencies of each type of system will be supported with the implemented filter structure at very low frequencies.

**Table 1.** Characteristics of the basic filter and class n frequency agile filter structure, [11].

| | *Main Circuit* | *Class n Frequency Agile Filter* |
|---|---|---|
| Center Frequency | $f_0 = 1/2\pi\sqrt{b}$ | $f_{0A} = \sqrt{(1-Ad^n)}f_0$ |
| Q-Factor | $Q = \sqrt{b}/a$ | $Q_A = \sqrt{(1-Ad^n)}Q$ |
| BP Gain | $G_{BP} = d^n/a$ | $G_{BPA} = G_{BP}$ |
| BP: -3dB Bandwidth | $\Delta f = a/2\pi b$ | $\Delta f_A = \Delta f$ |
| LP Gain | $G_{LP} = d^n$ | $G_{LPA} = G_{LP}/(1-Ad^n)$ |

For the implementation of a multi-protocol GPS filter structure, after careful search and investigation period, a $4^{th}$ order class 2 band pass filter implementation is selected. Targeted structure is given in Figure 19. The designed circuit is built of four cascaded main stages given in Figure 20.

In the implemented structure, number of feedback paths depend on the number of frequency ranges to be supported. In this structure, each parallel feedback circuit configured with same feedback currents and switches which enables to switch to any arranged center frequency by turning on the related feedback path.

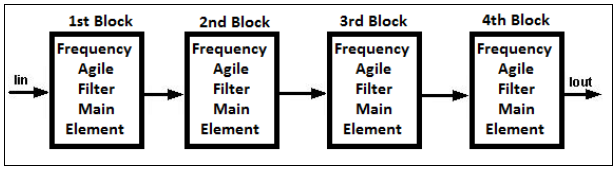


**Figure 19.** $4^{th}$ order frequency agile filter structure.

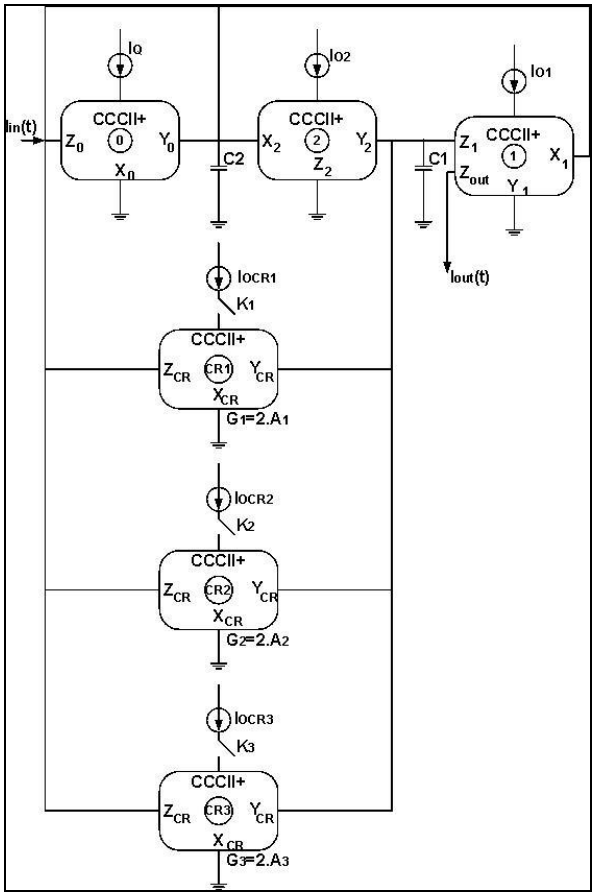


**Figure 20.** Main building block used in filter design, [12].

### 4.2. Simulation Results of the Designed Filter Structure

Gain adjustment currents are selected equally to set pass band gain at 0dB level in the implemented structure. In addition to this, biasing currents are selected as 10µA for the CCCII blocks in the filter stages. Each cases of filter responses when the feedback line is off and the cases for each triggered feedback kine to various center frequencies are shown in Figure 21.

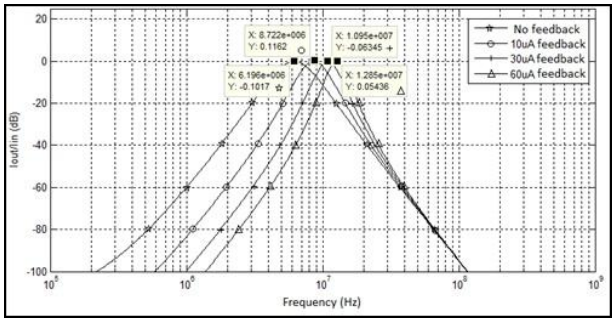


**Figure 21.** A closer look to frequency response of 4th order class 2 filter with dedicated current feedbacks.

In the designed filter structure, 4 different frequency filtering responses observed for; feedback line off (⌬) 6.14MHz, for 10µA feedback line (○) 8.60MHz, for 30µA feedback line (+) 10.94MHz and for 60µA feedback line open (Δ) 12.85MHz. Observed gain adjustment currents for these cases are; 13.5µA, 14.4µA, 16.5µA and 17.2µA. By selecting feedback currents at different levels, it is also possible to support higher or lower frequency filtering responses. In parallel to all characteristics, power consumption of the circuit is observed as 34.08µW.

## 5. Conclusion

In this work, a differential input pair based CCCII structure is realized and its application of a frequency agile, configurable filter structure is implemented. In overall design flow, behaviors of the designed circuit is exercised with the related simulations and shown for the appropriate operation. It is very clearly shown that the designed circuit is a great candidate solution to replace its recent discrete rivals being implemented in current designs. This study is an extended and improved version of a previous work and it is also important that to be the first implementation of such circuit in 28nm process design kit and to test the today`s supply and operating conditions.

## 6. Acknowledgement

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## 7. References

[1] Armagan E., "Design Examples for Second Generation Current Controlled Current Conveyors and Their Applications in 28nm Process" M. S. thesis, Graduate School of Engineering and Technology, Dept. of Electronics Engineering, ITU, Istanbul, Turkey, 2013.

[2] Armagan E., and Kuntman H., "Design of Balanced Differential Pair Based CCCII Circuit and Configurable Frequency Agile Filter Application in 28nm Process", ELECO 2012, Symposium of Electrical-Electronics and Computer Engineering, Bursa, Turkey, 2012.

[3] Armagan E., and Kuntman H., "Configurable Frequency Agile Filter Application of Balanced Differential Pair Based CCCII Circuit in 28nm Process", LASCAS 2013, 4th IEEE Latin American Symposium on Circuits and Systems, Cusco, Peru, 2013.

[4] Mak P., Seng-Side U, Rui P. M., "Transceiver structure selection: Review, State-of-the-art survey and case study", *IEEE Circuits and Systems Magazine*, Vol 7., Issue 2., pp. 6 - 25, 2007.

[5] Razavi B., "RF Microelectronics", *Prentice Hall*, ISBN: 978-0128875718, 1997.

[6] Sun Y, "Generalized Bandpass Sampling Receivers for Software Defined Radio", *Doctoral Thesis*, Royal Institute of Technology, ICT, Stockholm, Sweden, 2006.

[7] Mitola J., "The software radio architecture", *IEEE Comm. Magazine*, Vol. 33, No. 5, pp. 26 - 38, 1995.

[8] Kurashina T., Ogawa S., Watanbe K., "A CMOS Rail-to-Rail Current Conveyor", *IEICE Trans Fundamentals*, Vol. E85-A, No. 12, pp. 2894 – 2900, 2002.

[9] Fabre A., Saaid O., Wiest F., Boucheron C., "High Frequency Applications Based on a New Current Controlled Conveyor", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 43, No. 2, pp 82 – 91, 1996.

[10] Chipipop B., Chaisricharoen R., Sirinaovakul B., "A novel balanced differential-pair multi-output CMOS CCCII", *Industrial Electronics and Applications*, 2008, pp 351 – 356.

[11] Chipipop B., Chaisricharoen R., Sirinaovakul B., "A balanced differential-pair CMOS CCCII with negative intrinsic resistance", *IEEE Signals, Circuits and Systems International Symposium*, 2009, pp 1 – 4.

[12] Lakys Y., Godara B., Fabre A., "Cognitive and encrypted communications: state of the art and a new approach for frequency-agile filters", Turk J Elec Eng & Comp Sci, Vol.19, No:2, 2011, pp 251 – 273.

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