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A Common-Gate, g_m-boosting LNA Using Active Inductor-Based Input Matching for 3.1–10.6 GHz UWB Applications

Humirah Majeed, Vikram Singh

School of Electronics and Communication Engineering, Shri Mata Vaishno Devi University, Katra, Jammu & Kashmir, India

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ABSTRACT

This paper presents the circuit of a low-noise amplifier (LNA) using active inductor (AI) input matching with common gate (CG) current-reused technique. This configuration is implemented in 90 nm CMOS and enables to achieve high power-gain (S_{21}) with ultra-wideband (UWB) input matching at low power levels. Utilization of modified high-Q AI at the input side of the proposed LNA reduces the number of inductors and achieves UWB from only two inductors. Proposed LNA dissipates 10.4 mW from 1.0 V supply and exhibits an S_{21} response of 18.0 ± 0.8 dB for 3.1–10.6 GHz with a maximum and average S_{21} of 18.8 dB and 18.22 dB, respectively. The proposed LNA has noise-figure (NF) equal to 3.36–4.68 dB, with input (S_{11}) and output (S_{22}) reflection coefficients of less than −9.3 dB and −11.35 dB, respectively across the entire UWB range.

Index Terms—Active-inductor, common-gate, current-reuse, low noise amplifier, UWB

I. INTRODUCTION

Due to the demand for high data rates in wireless communication, ultra-wideband (UWB) technology has attracted great attention. Demand for a high data rate can be achieved using UWB technology as it consumes very less power and requires less complex receiver architectures [1,2]. Not only this, nowadays, every communication media ranging from TV receiver to telephone receiver has changed from wired to wireless and every wireless communication system needs one or other form of transceiver circuit which consists of a low-noise amplifier (LNA) as a first active key component [3-7]. The signal which an LNA receives from antenna needs to be amplified by the LNA without adding much noise to it. The overall performance of a receiver circuit depends upon the sensitivity of the LNA circuit and it has to satisfy various parameters such as low-noise figure (NF), high power gain (S_{21}), wideband input (S_{11}) and output (S_{22}) matching, high linearity, and unconditional stability.

In order to accomplish all these objectives, different LNA topologies have been proposed by many researchers and each of these topologies have a trade-off between various performance parameters. Based upon complementary metal-oxide semiconductor (CMOS) configurations, common source (CS) [4,5,8-12] and common gate (CG) [6,7,13-18] are the two broad categories in which these LNAs can be classified. These topologies are shown in Fig. 1. Common source resistive termination (CS-RT) LNA can be used for wideband impedance matching but at the cost of high NF, as a resistor at the input of the transistor adds thermal noise to the signal [5]. Feedback LNA achieves wideband impedance matching with an NF better than CS-RT as the signal is not attenuated with the noisy resistor before amplification [4]. For example, LNA presented in [8] achieves 12.4 dB S_{21} with NF of 2.7–3.7 dB. Common source inductive degeneration (CS-ID) topology provides high S_{21} with low NF and good input matching for narrowband applications [19,20]. Distributed LNA employs several parallel transistors to achieve extreme wideband input matching and provides small additive gain and high NF as reported in [21,22].

Common gate LNA renders a fairly higher NF as compared to CS amplifiers and a large area is occupied by the inductors used. However, it shows wideband behavior due to its simple and easy achieve input impedance matching by maintaining the transconductance of input

Corresponding author: Vikram Singh
E-mail: vikram.singh@smvdu.ac.in
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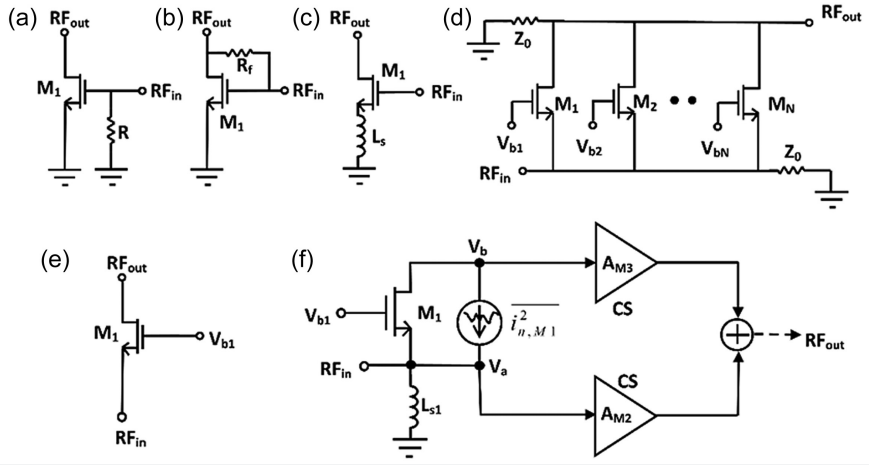

Fig. 1. LNA topologies: (a) common source resistive termination, (b) feedback LNA, (c) common source with inductive degeneration, (d) distributed LNA, (e) common gate LNA, (f) CG-CS noise-canceling LNA.

CG transistor close to 20 mS [14]. Common gate followed by CS (CG-CS) noise-canceling technique shown in Fig. 1(f) utilized in [23-25] is still unable to resolve the problem of large chip area. Several methods have been utilized to decouple the trade-off between NF and impedance matching, but the trade-off has not been fully decoupled.

For the matching network, most of the LNAs use bulky passive inductors requiring several hundred micrometers of interconnects. These passive inductors also possess fixed inductance values and poor quality factors [26]. Thus, to reduce the chip area, active inductor LNA topologies have been used in [27-29]. The active inductors are advantageous in the sense that they have tunable inductance value, less cost and high-quality factor, and smaller chip area. An LNA architecture employing active inductor for the input matching is presented in this paper.

The rest of this manuscript is organized as follows: In Section II, the g_m-boosting mechanism and active inductor are discussed. Section III discusses the proposed LNA circuit and its operation. Input impedance, output impedance, and stability of the proposed LNA are also analyzed in Section III. The results for the proposed LNA are discussed in Section IV. Finally, Section V concludes this manuscript.

II. METHODOLOGY ADOPTED

A. G_m-Boosting Mechanism in LNA

Common gate configuration with g_m-boosting technique is implemented to design an LNA with high gain over the entire UWB besides dissipating very less power. There is a tight coupling between NF characteristics and input impedance matching of CG-LNA. To enhance the performance and to overcome its drawbacks, g_m-boosting technique is a decent choice. The NF of CG-LNA is restricted by $1/g_m$ and thus can be decreased by increasing the transconductance (g_m). At the other aspect, for input matching R_s ($\approx 1/g_m$) is set to 50 Ω. Because of the input matching condition, $g_m R_s = 1$, it is not favorable to increase the transconductance randomly in order to reduce the noise factor as the noise factor has an inseparable link with input matching condition. However, by employing the g_m-boosting technique, the *NF* performance can still be improved by decoupling the input matching and noise figure.

Fig. 2, shows a CG-LNA with g_m-boosting. An amplifier with negative gain ($-A$), when inserted between the source and gate terminal of the input CG-stage, will increase the overall transconductance. The input signal is applied to the gate of transistor M_1 after being amplified by a gain of $-A$ by the inverting gain block; hence, the transconductance of the CG amplifier is increased by $(1+A)$ times.

The input matching condition becomes $(1+A)\ g_m R_s = 1$, thereby reducing the NF by a factor of $(1+A)$, relaxing the stringent requirements on the noise factor. The channel noise of input transistor in g_m-boosted CG-LNA is less because it requires a lower bias current. In Fig. 2, the inverting gain is achieved by using a CS amplifier.

B. Active-Inductor (AI)

Although passive spiral inductors have a wide variety of applications, they suffer from a number of disadvantages as well. The major disadvantages of passive inductors are limited inductance value and simultaneously have low self-resonance frequency which is non-tunable. Low-quality factor (Q) and large silicon area are another disadvantages of passive inductors. Contrarily, active inductors possess many important advantages such as reduced chip area requirement, high resonance frequencies with high tunable Q, and inductance value.

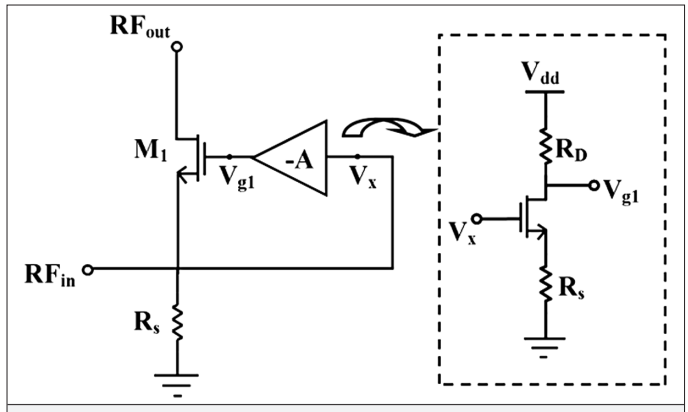

Fig. 2. Common gate-LNA with g_m-boosting.

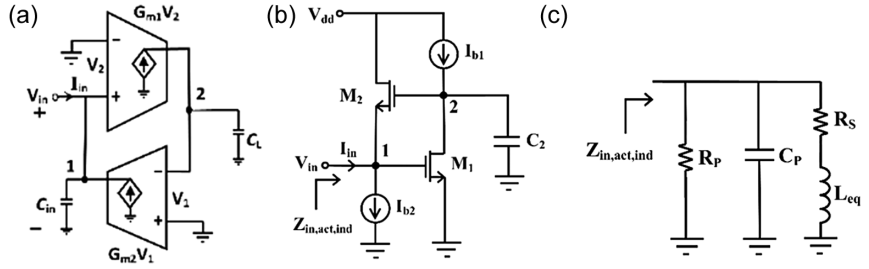

Fig. 3. Gyrator-C-based active inductor, (a) block diagram, (b) schematic diagram, (c) equivalent circuit.

The block diagram of a gyrator-based AI with its schematic as shown in Fig. 3 is utilized in the proposed LNA circuit and it consists of a positive and a negative transconductance amplifiers connected back to back [26].

In this active inductor, after biasing through the current sources I_{b1} and I_{b2}, the transistor M_1 provides negative transconductance, whereas the transistor M_2 provides positive transconductance. This circuit converts capacitance C_2 which includes gate-drain parasitic capacitance of M_2 and other parasitic capacitances into its equivalent active inductor as shown in Fig. 3(c). The input admittance ($Y_{in,act,ind}$) then can be expressed as

$$Y_{in,act,ind} = \frac{1}{Z_{in,act,ind}} = sC_P + \frac{1}{R_P} + \frac{1}{R_S + sL_{eq}} \tag{1}$$

where

$$C_p = C_{gs1}; \quad R_p = \left(g_{ds1} + g_{m2}\right)^{-1}; \quad R_s = g_{ds2}\left(g_{m1}g_{m2}\right)^{-1}; \quad L_{eq} = C_2\left(g_{m1}g_{m2}\right)^{-1} \tag{2}$$

The drain-source output conductances at node 1 and 2 are given by g_{ds1} and g_{ds2}, respectively. Solving for the self-resonating frequency (ω_0) and quality factor (Q) of the active-inductor in (3) and (4) as

$$\omega_0 = \sqrt{\frac{1}{C_p L_{eq}} - \frac{R_s^2}{L_{eq}^2}} \approx \sqrt{\frac{1}{C_p L_{eq}}} \quad \text{(for small } R_s\text{)} \tag{3}$$

and

$$Q = \frac{R_p\left[\omega L_{eq} - \omega C_p(R_s^2 + \omega^2 L^2)\right]}{(R_s^2 + \omega^2 L^2) + R_s R_p} \approx \begin{cases} \dfrac{R_p}{\omega L_{eq}}, & \text{for } R_p >> R_s \\ \dfrac{\omega L_{eq}}{R_s}, & \text{for } R_s >> R_p \end{cases} \tag{4}$$

For achieving good quality, high Q in high value of R_p and small value of R_s are always expected from the active inductor. The active inductor circuit utilized at the input of the proposed LNA is shown in Fig. 4a, where C_2 here includes gate-drain parasitic capacitances of M_2 and M_3, respectively. The ideal current sources I_{b1}, I_{b2}, and I_{b3} are replaced by MOS current sources in final circuit and this will reduce the value of series resistance R_s and increase the equivalent inductance L_{eq}.

From small signal equivalent of the active inductor used in this LNA is shown in Fig. 4b, the equivalent values for C_p, R_p, R_s, and L_{eq} can be approximated as:

$$C_p \approx C_{gs1};\ R_p \approx \frac{1}{g_{ds2}};\ R_s \approx \frac{g_{ds1}g_{ds3}}{g_{m1}g_{m2}g_{m3}};\ L_{eq} \approx \frac{sC_{gs2}}{g_{m1}g_{m2}} \tag{5}$$

where g_{ds1}, g_{ds2}, and g_{ds3} are the drain-source conductance of transistor M_1, M_2, and M_3, respectively. From equation (5), it is clear that L_{eq} is inversely proportional to g_{m1} and g_{m2}. Now, using equations (3), (4), and (5), the resonant frequency and the quality factor (Q) of the active inductor shown in Fig. 4a can be expressed as

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}};\ Q = \sqrt{\frac{g_{m1}g_{m2}g_{m3}^2C_{gs2}}{g_{ds1}^2g_{ds3}^2C_{gs1}}} \tag{6}$$

It is clear from equation (6) that the resonant frequency of the active inductor shown in Fig. 4 is directly proportional to g_{m1} and g_{m2}, whereas its Q-factor is directly proportional to g_{m1}, g_{m2}, and g_{m3}. The variation in Q-factor with frequency for the active inductor used in this LNA is shown in Fig. 4(c) and it achieves a minimum Q-factor of 7.3 for 3.1–10.6 GHz frequency range.

III. PROPOSED ACTIVE INDUCTOR-BASED LNA

The proposed g_m-boosted active inductor-based LNA with CG as input stage is shown in Fig. 5. The active inductor topology here is used for input-impedance matching whereas the CG topology with g_m-boosting is employed here for achieving high gain and low NF over the UWB frequency range.

The input matching network is designed using a gyrator-C-based AI realized by transistors M_1, M_3 forming positive transconductance and biased using current sources I_{b1} and I_{b3}, whereas M_2 is forming negative transconductance and biased using I_{b2}. The active inductor is connected in conjugation with the CG stage to achieve the matching condition. The transistor M_5 is in CG mode and the inverting gain block is realized using CS transistor M_4. The transistor M_4 is connected between the gate-to-source terminal of CG transistor M_5, thus boosting its transconductance by a factor of $A \approx g_{m4}R_2$ without increasing the bias current. Increasing the transconductance by A times, the noise factor is reduced by the same amount thus decoupling the noise factor and input matching characteristics. The effect of adding g_m-boosting transistor M_4 on S_{21} and NF is shown in Fig. 6. Also, the CG configuration reduces the miller effect and provides a better isolation to the output signal and a noise factor relatively independent of frequency. The bias network of M_4 comprises of gate biasing resistor R_1 and the coupling capacitor C_1. Similarly, the resistor R_3 and capacitor C_3 form the bias network of M_5.

The output of M_5 is loaded by LC tank in which inductor L_1 is tuned with gate-drain capacitance of M_5. Signal matching from stage-1 to stage-2 is achieved by another serially tuned LC tank formed by inductor L_2 and gate-source parasitic capacitance C_{gs6} of successive gain-stage formed by transistor M_6.

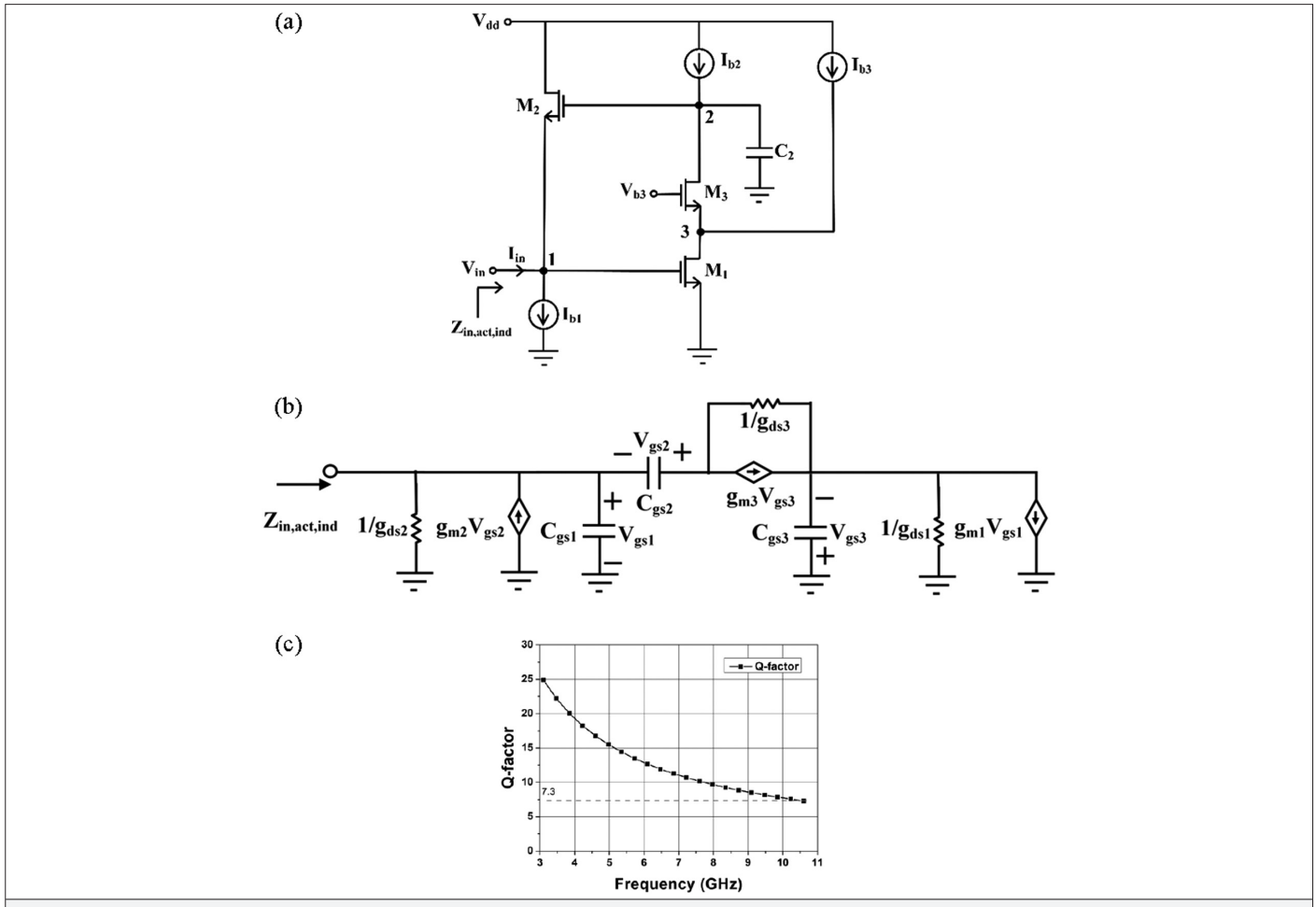

Fig. 4. (a) Circuit diagram of high-*Q* active inductor, (b) small-signal equivalent, and (c) Q-factor performance.

Transistor M_7 acts as the buffer stage with the current source load being modeled by M_8 and the biasing resistance R_7. The individual elements used in the proposed LNA with their values are listed in Table I.

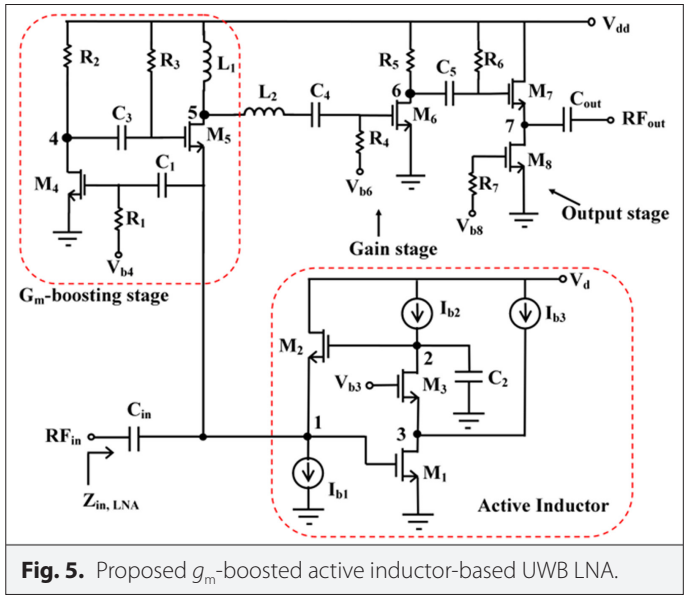

Fig. 5. Proposed g_m-boosted active inductor-based UWB LNA.

A. Circuit Analysis of Proposed

1) Input Matching Analysis

As is well known, the input impedance of the LNA should be matched with the source impedance R_s for maximum power transfer and least reflections, where R_s is the receiver's antenna resistance. The simplified small-signal equivalent circuit of the input stage for calculating input impedance of the proposed LNA is shown in Fig. 7. For small-signal analysis, the biasing capacitors C_1 and C_3 are considered as short-circuited. The resistance R_{eq} shown in Fig. 7 is parallel combination of $1/g_{ds4}$, R_2 and R_3 (i.e., $R_{eq} = ((1/g_{ds4})||R_2||R_3)$.

The input impedance of the proposed LNA can be approximated as:

$$Z_{in,LNA} \approx Z_x \left|\right| \left(Z_{in,act,ind} \left|\right| \frac{1}{j\omega C_{gs4}} \right) \tag{7}$$

where $Z_{in,act,ind}$ is the total impedance of the active inductor, C_{gs4} is the gate-to-source capacitance of M_4, and impedance Z_x is given by:

$$Z_x = \frac{V_x}{I_x} = \frac{1 + Z_{load} g_{ds5}}{g_{m5} + g_{ds5}} \tag{8}$$

where g_{m5} is the transconductance of M_5 and Z_{load} is the load impedance. The input reflection coefficient (S_{11}), which is a function of input impedance $Z_{in,LNA}$ and source resistance R_s, is given by:

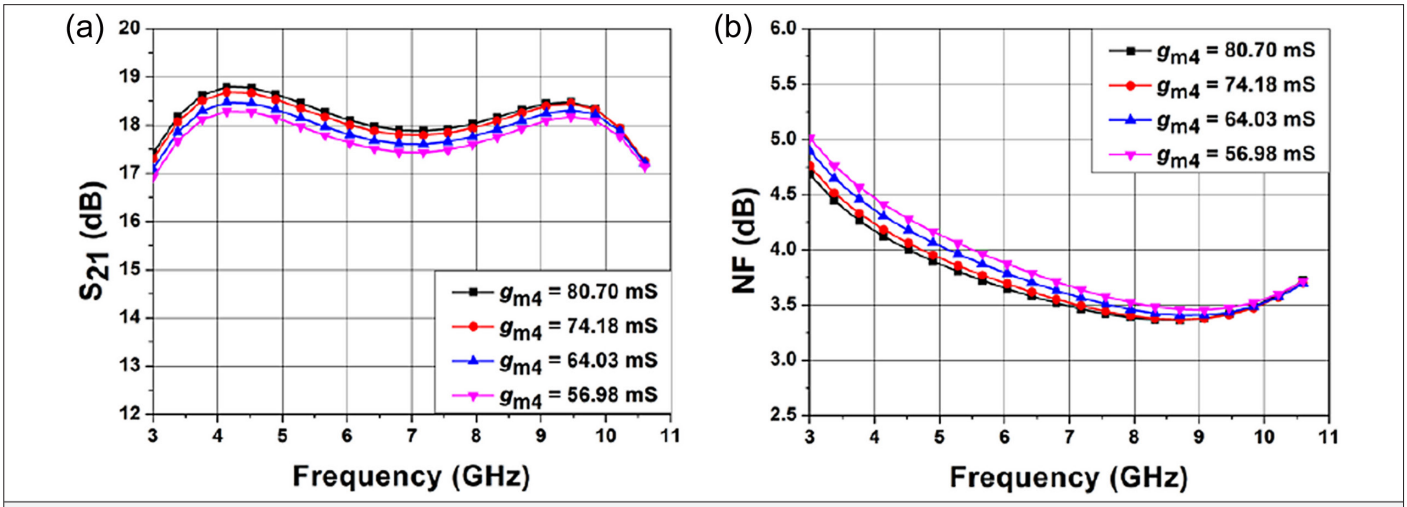

Fig. 6. Effect of g_m-boosting transistor M_4 on (a) S_{21} and (b) NF.

TABLE I. COMPONENTS FOR THE PROPOSED AI-BASED LNA CIRCUIT

Transistors, W (μm)/L (μm)		Resistors (kΩ)		Capacitors (pF)		Inductors (nH)	
M_1, M_3	1/0.09	R_1, R_3, R_7, R_6	5.0	C_{in}, C_1, C_3	10	L_1	10
M_2	5/0.09	R_4	0.60	C_4	6.8	L_2	10
M_4	105/0.09	R_2	0.05	C_5	2.0		
M_5, M_7, M_8	30/0.09	R_5	0.43	C_{out}	10		
M_6	20/0.09						

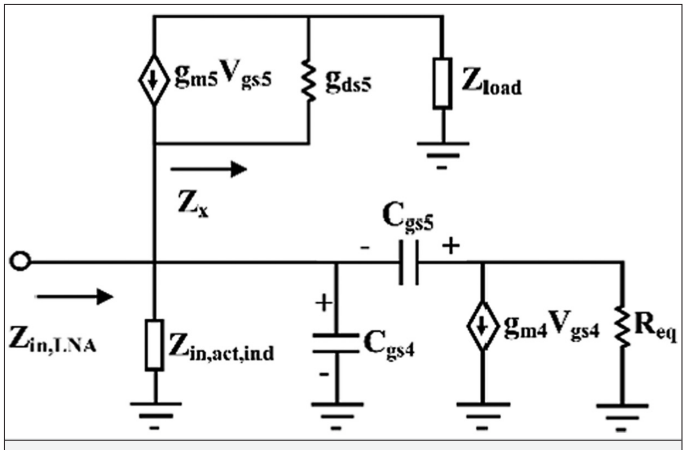

Fig. 7. AC equivalent of the input stage.

$$S_{11}=\frac{Z_{in,LNA}-R_s}{Z_{in,LNA}+R_s} \tag{9}$$

The major portion of wideband input matching is provided by the $1/g_{m5}$, whereas the rest is contributed by the input impedance of active inductor and the g_m-boosting stage. The input imedance matching (S_{11}) for different values of g_{m1}, g_{m4}, and g_{m5} is shown in Fig. 8 from which it is depicted that transistor M1 of AI and transistor M4 of input CG-stage are playing an important role in achieving UWB input matching.

2) Output Matching Analysis

Another issue responsible for achieving a good LNA circuit design is output impedance matching which can be defined using output reflection coefficient (S_{22}). The ac equivalent of the output buffer stage is shown in Fig. 9.

Exploiting the ac analysis of output stage, the output impedance ($Z_{out,LNA}$) is given by:

$$Z_{out,LNA}=\frac{V_{out}}{I_{out}}=\frac{r_{ds7}\,\|\,r_{ds8}\,\|\left(j\omega C_{gs7}\right)^{-1}}{1+g_{m7}\left(r_{ds7}\,\|\,r_{ds8}\,\|\left(j\omega C_{gs7}\right)^{-1}\right)} \tag{10}$$

where $r_{ds7}=(g_{ds7})^{-1}$, $r_{ds8}=(g_{ds8})^{-1}$, g_{m7}, and C_{gs7} are transconductance and gate-to-source parasitic capacitance of M_7 and M_8, respectively and then S_{22} can be expressed as:

$$S_{22}=\frac{Z_{out,LNA}-R_s}{Z_{out,LNA}+R_s} \tag{11}$$

C) Noise Analysis

For the NF analysis, the small-signal noise equivalent circuit of the proposed LNA is shown in Fig. 10, where the drain-induced channel thermal noise is considered as the main source of noise in transistors used in active inductor and the CG current reused.

Absolutely, the noise added by the active inductor at node1 cannot be ignored; therefore, the total root-mean-square (rms) noise voltage due to active inductor circuit at node1 can be represented as:

$$\overline{V_{n,out,act,ind}^2}=\overline{V_{n,d1}^2}+\overline{V_{n,d2}^2}+\overline{V_{n,d3}^2} \tag{12}$$

where, $\overline{V_{n,dx}^2}$ represents noise voltage due to M_1, M_2, and M_3, respectively. If $\overline{V_{n,out,Rs}^2}$ is the output noise due to source resistance R_s, then Eq. (12) can be expressed as:

$$\overline{V_{n,out,act,ind}^2}=R_s\left\{\left(\frac{g_{m2}g_{m3}}{g_{m3}+g_{o3}}\right)^2\frac{\gamma}{\alpha\left|sC_2+g_{o2}\right|^2}\left(g_{m1}+g_{m3}\right)+\frac{\gamma g_{m2}}{\alpha}\right\}\overline{V_{n,out,Rs}^2} \tag{13}$$

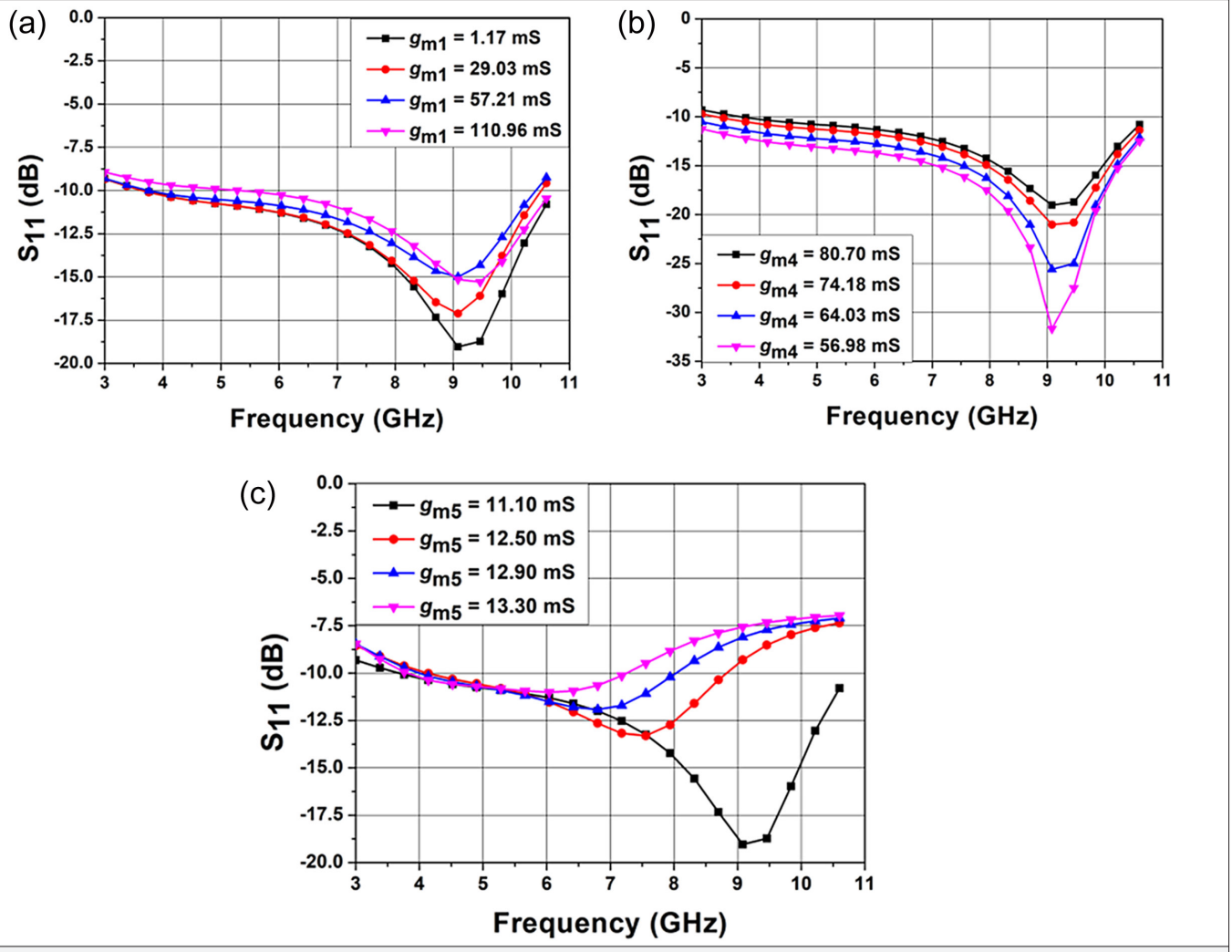

Fig. 8. Input reflection coefficient ($_{S11}$): (a) effect of g_{m1}, (b) effect of g_m-boosting, and (c) effect of input common-gate stage.

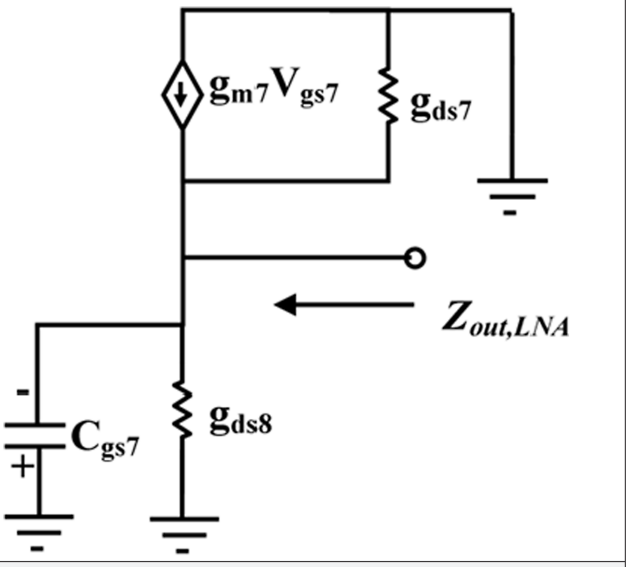

Fig. 9. AC equivalent of the buffer stage.

The output noise due $\overline{i_{n,d5}^2}$ and $\overline{i_{n,d4}^2}$ can be expressed as:

$$\overline{V_{n,out,ind5}^2} = \frac{\gamma}{\alpha}\left|\frac{1}{R_s}+\frac{1}{Z_{in,act,ind}}\right|^2 \times \frac{R_s\overline{V_{n,our,Rs}^2}}{g_{m5}(1+A)^2} \quad (14)$$

and

$$\overline{V_{n,out,ind4}^2} = \frac{K^2}{P^2}\frac{\gamma g_{m4}}{\alpha R_s}\overline{V_{n,out,Rs}^2} \quad (15)$$

respectively. Whereas the noise due to $\overline{V_{n,R2}^2}$ is given by:

$$\overline{V_{n,out,R2}^2} = \frac{K^2R_2}{P^2R_s}\times\overline{V_{n,out,Rs}^2} \quad (16)$$

where, $\overline{V_{n,out,Rs}^2} = P^2\overline{V_{n,Rs}^2}$;

$$K = \left[R_2\left(\frac{1}{R_2g_{m5}}\left(\frac{1}{R_s}+\frac{1}{Z_{in,act,ind}}+g_{m5}\right)+g_{m4}\right)\left(\frac{1}{R_s}+\frac{1}{Z_{in,act,ind}}\right)\right]^{-1}$$

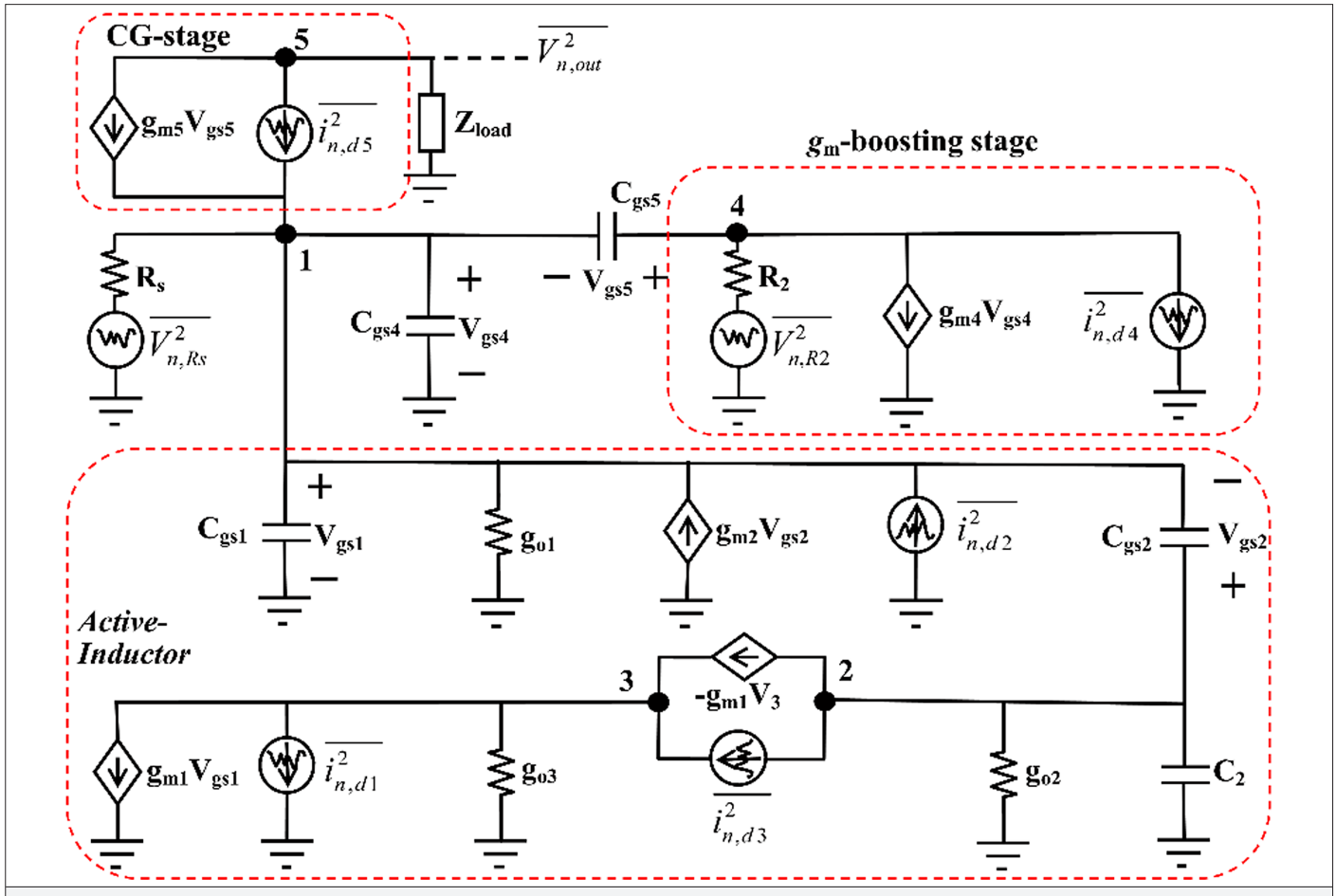

Fig. 10. Small-signal noise equivalent circuit of AI-based LNA.

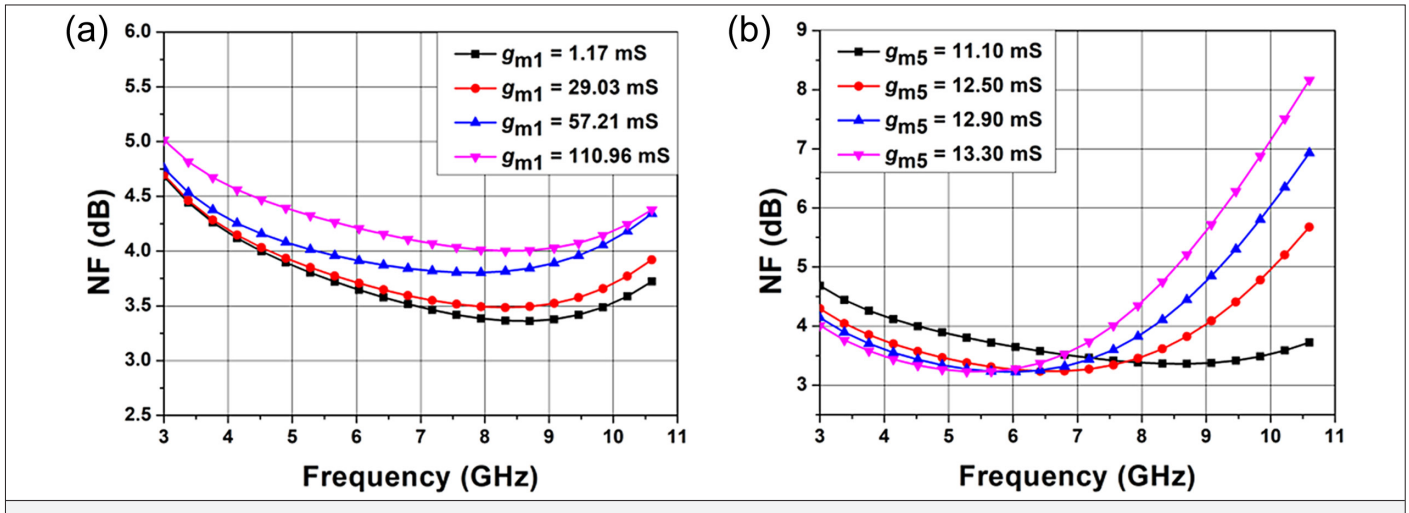

Fig. 11. Variation in NF: (a) with g_{m1}, (b) g_{m5} of input common gate stage.

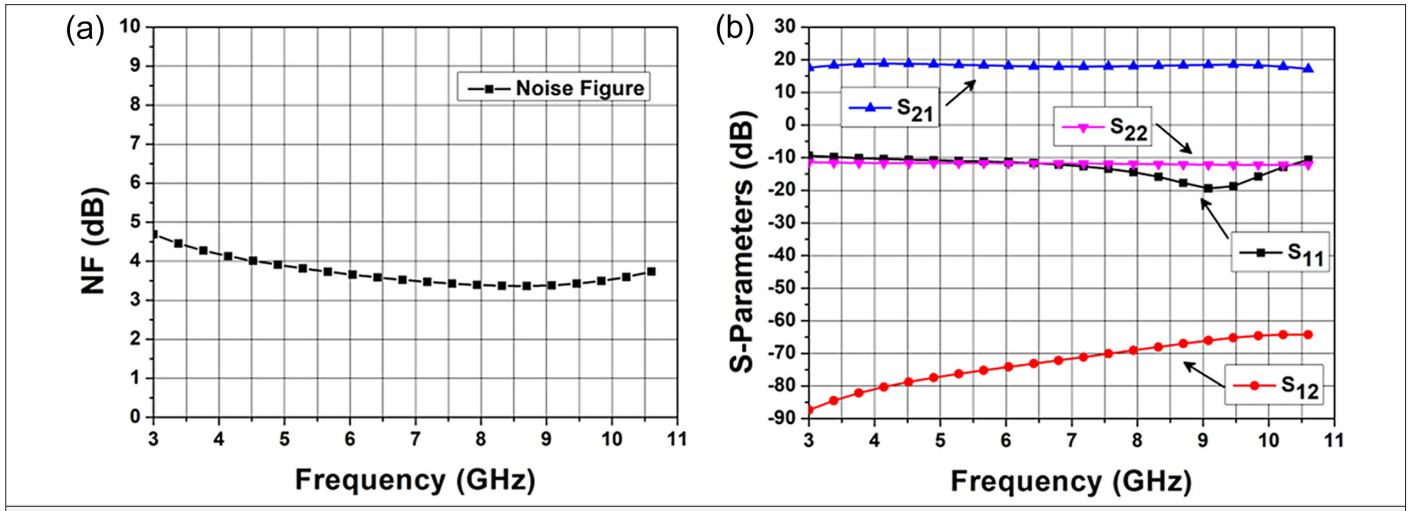

Fig. 12. LNA characteristics: (a) noise-figure and (b) S-parameters.

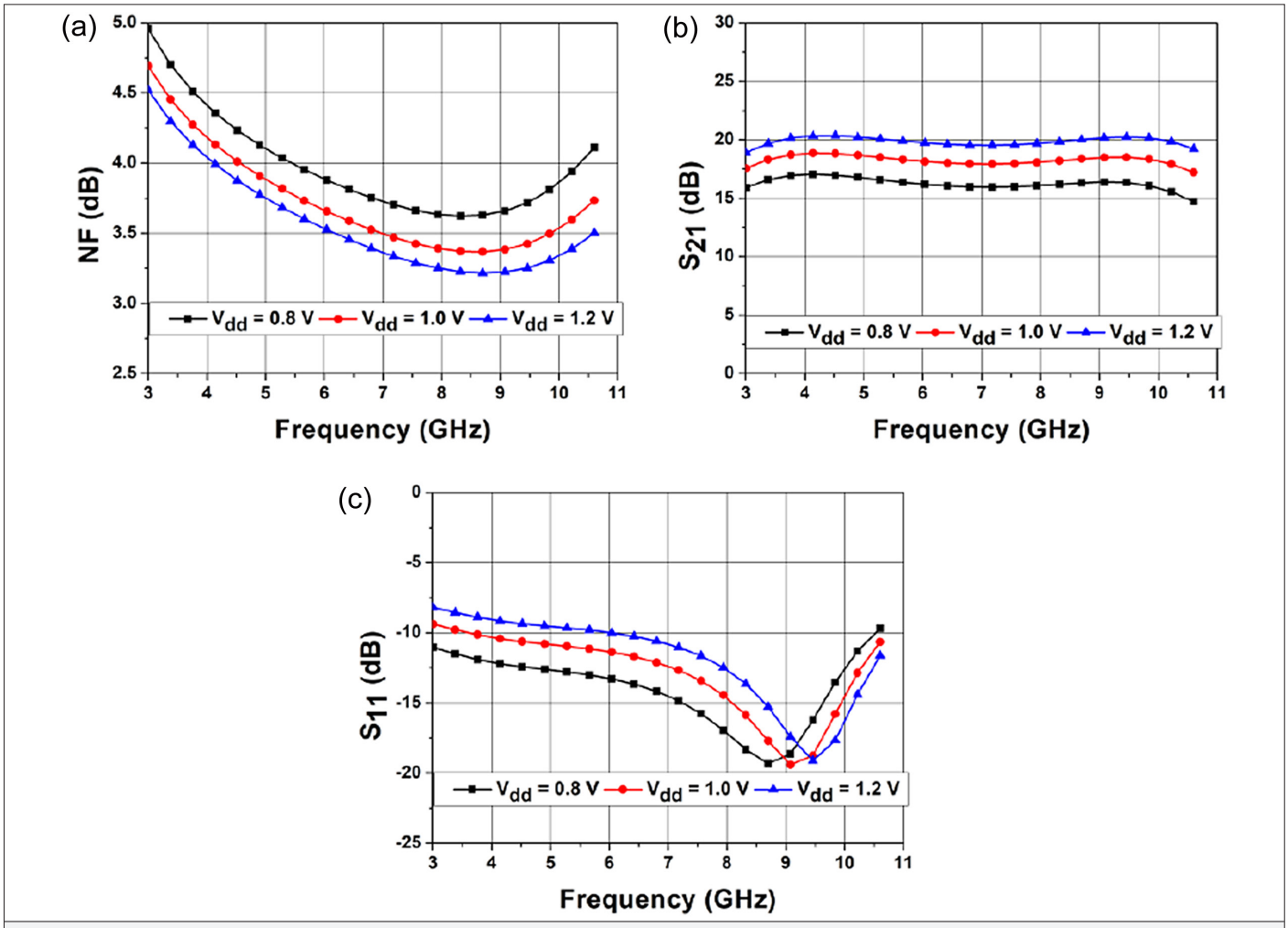

Fig. 13. (a) NF, (b) S_{21}, and (c) S_{11}, at various V_{dd} supply.

and

$$P = \frac{g_{m5}(1+A)}{R_s\left(\frac{1}{R_s}+\frac{1}{Z_{in,act,ind}}+g_{m5}(1+A)\right)}$$

Therefore, the NF of the proposed LNA can be expressed as:

$$NF \approx 1+R_s\left\{\left(\frac{g_{m2}g_{m3}}{g_{m3}+g_{o3}}\right)^2\frac{\gamma}{\alpha\left|sC_2+g_{o2}\right|^2}\left(g_{m1}+g_{m3}\right)+\frac{\gamma g_{m2}}{\alpha}\right\} + \frac{\gamma}{\alpha}\left|\frac{1}{R_s}+\frac{1}{Z_{in,act,ind}}\right|^2\times\frac{R_s}{g_{m5}(1+A)^2}+\frac{K^2\gamma g_{m4}}{P^2\alpha R_s}+\frac{K^2R_2}{P^2R_s} \quad (17)$$

where γ and α are the coefficients of channel-induced thermal noise.

Equation (17) and Fig. 11 reveals that NF can be reduced by considering small-sized transistor for M_1 and large size for M_5. Antenna source resistance matching simultaneously with low NF can be achieved by a parallel combination of impedance due to feedback loop of M_4 and M_5, and input impedance of the active inductor (i.e., $Z_{in,act,ind}$).

IV. RESULTS AND DISCUSSION

The proposed g_m-boosting AI-based CG LNA was simulated using Cadence Spectre RF at a V_{dd} supply of 1.0 V. Fig. 12 shows the results of NF and S-parameters. It is observed that NF has a span of 3.36–4.68 dB with a power gain in the range of 17.22–18.79 dB over the UWB frequency range of 3.1–10.6 GHz. The achieved values for S_{11} and S_{22} are less than −9.31 dB and less than −11.35 dB, respectively. The proposed LNA is a suitable option for wireless local area network (WLAN) receivers as a flat gain response of 18.0 ± 0.8 dB with a minimum NF of 3.362 dB and excellent matching is achieved for the entire UWB frequency range. The NF of the proposed circuit is slightly higher due to the use of active inductor for input matching but it reduces the chip area. As the input RF signal is applied at the source terminal of input CG configuration, it results in a good reverse isolation of better than −64.36 dB for the entire bandwidth.

Fig. 13 shows the characteristics of the proposed AI-based LNA at 0.8 V, 1.0 V, and 1.2 V of V_{dd} supply. It has been observed that as supply voltage increases from 0.8 V to 1.2 V, the power gain increases, which decreases the value of NF but the input matching deteriorates. The value to NF varies from a minimum of 3.215 dB at V_{dd} equal to 1.2 V

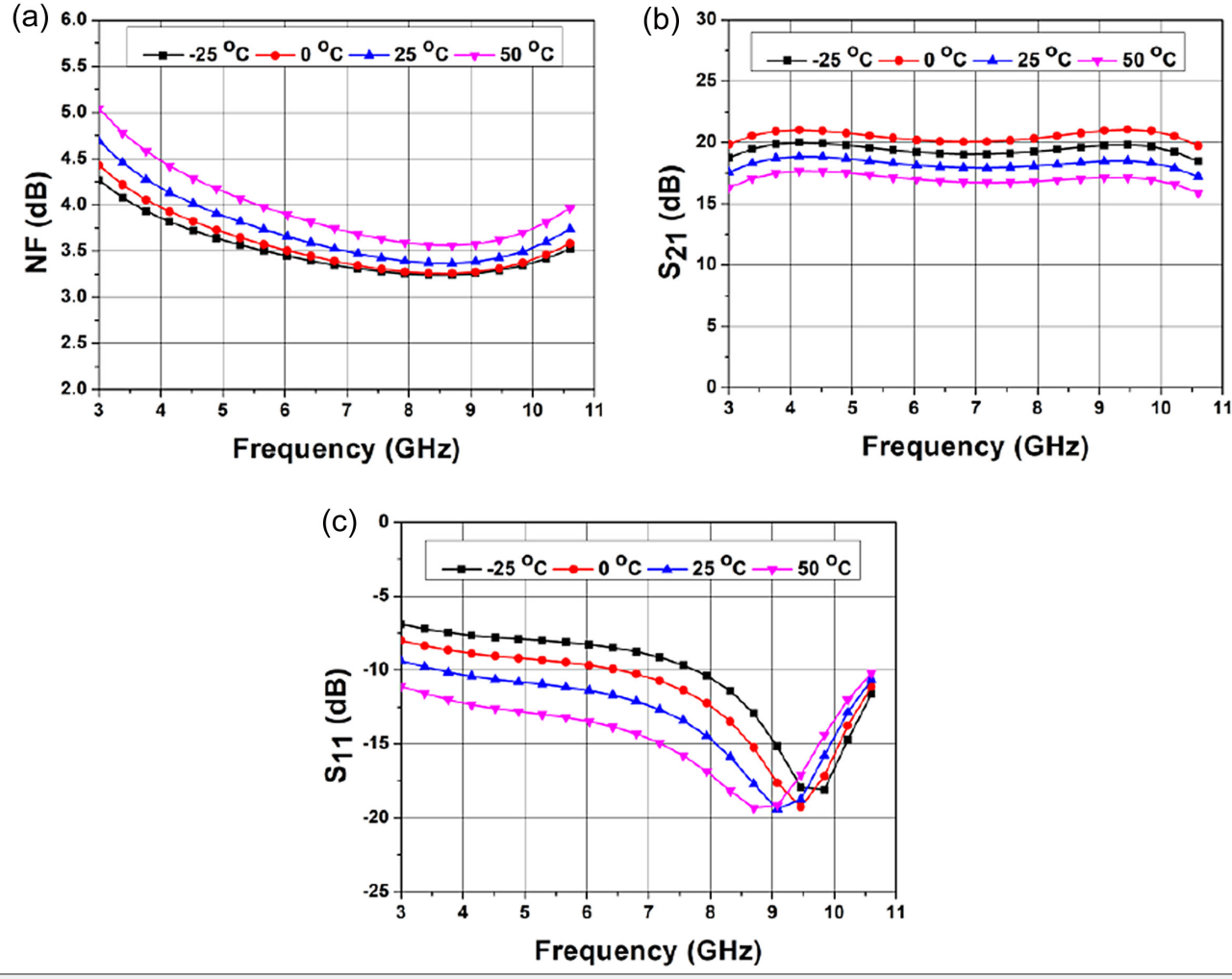

Fig. 14. (a) NF, (b) S_{21}, and (c) S_{11}, at different temperatures.

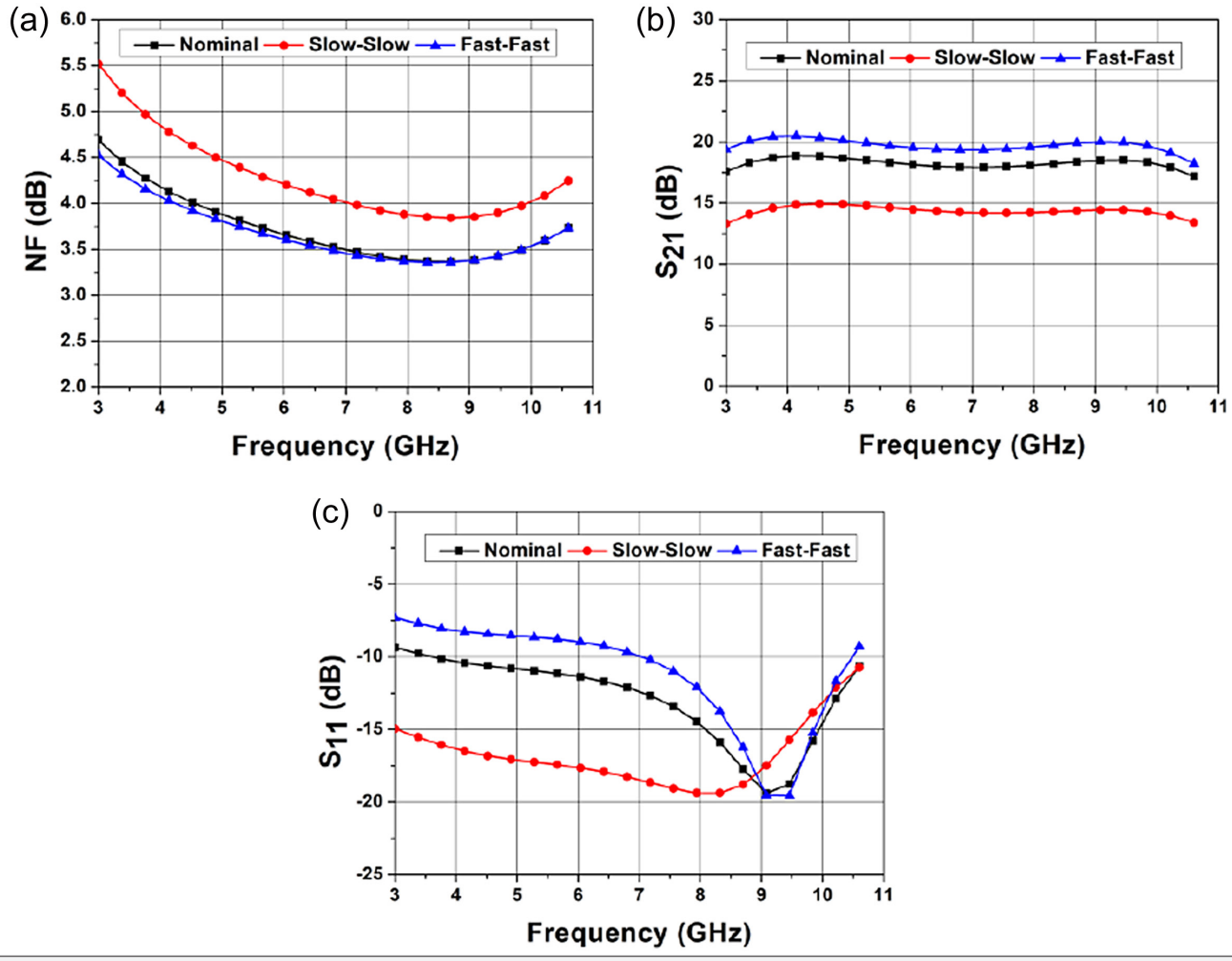

Fig. 15. Performance under process corner variation: (a) NF (b) S_{21}, and (c) S_{11}.

to a maximum of 4.958 dB at V_{dd} equal to 0.8 V, whereas S_{21} varies from 14.70 to 20.34 dB, with a standard deviation of 1.55 dB from its average value of 18.096 dB. The mininum value of S_{11} varies from less than −8.193 dB to less than −9.688 dB.

Further, it is always desired from a designed LNA that, with the change in operating temperature, the performance parameters should remain in the acceptable range. The stability of the system parameters NF, S_{21}, and S_{11} against temperature variation at different temperatures of −25°C, 0°C, 25°C, and 50°C is shown in Fig. 14. This LNA achieves NF of 3.24 dB at 25°C to 5.05 dB at 50°C and S_{21} greater than 15.90 dB and S_{11} less than −6.90 dB at different temperatures. The extremes of the parameter variations within which a circuit must function properly can be represented by process corners. Fig. 15 shows NF, S_{21}, and S_{11} at different process parameters with a comparison with LNA discussed in this paper. Due to process variation, NF varies from 3.35 to 5.52 dB, minimum S_{21} varies from 13.28 dB to 18.22 dB, and S_{11} of less than −7.3 dB.

The linearity performance of the proposed LNA is observed in terms of 1-dB compression point (P_{1dB}), the power gain and the output signal power at P_{1dB}, third-order intercept point (IIP_3), and the second-order intercept point (IIP_2). The linearity performance plots for the proposed LNA are shown in Fig. 16. The simulated 1-dB compression point of the proposed LNA is approximately −32.3 dBm with a flat gain of approximately 17.1–18.1 dB. The proposed LNA provides an output signal power (P_{out}) of −15.3 dBm at P_{1dB} as shown in Fig. 16(c). Two-tone test is performed at center frequency of 6 GHz with $f_1 = 5.995$ GHz and $f_2 = 6.005$ GHz spaced at 10 MHz in order to analyze IIP_3. The simulated IIP_3 for the proposed LNA was found to be −22.8 dBm as can be seen from Fig. 16(d). For a UWB LNA, it is also important to analyze second-order linearity in case of direct-conversion type receiver architectures. The simulated IIP_2 of the proposed LNA is −16.8 dBm as shown in Fig. 16(e).

The phase linearity of the proposed LNA is observed in terms of group-delay variations. Due to the presence of two large-sized inductor, the proposed LNA achieves a group delay of 85.60 ± 25.2 ps for 3.1–10.6 GHz frequency range and is found comparable with the other LNAs reported in [16,20] as shown in Fig. 17.

The oscillations occur at the output of the LNA if the system is not stable. So stability is an important performance parameter. The LNA should be unconditionally stable over the entire bandwidth which can be analyzed by using Rollett's stability factor (K). For a system to be stable, it should satisfy the conditions expressed by equations (18) and (19):

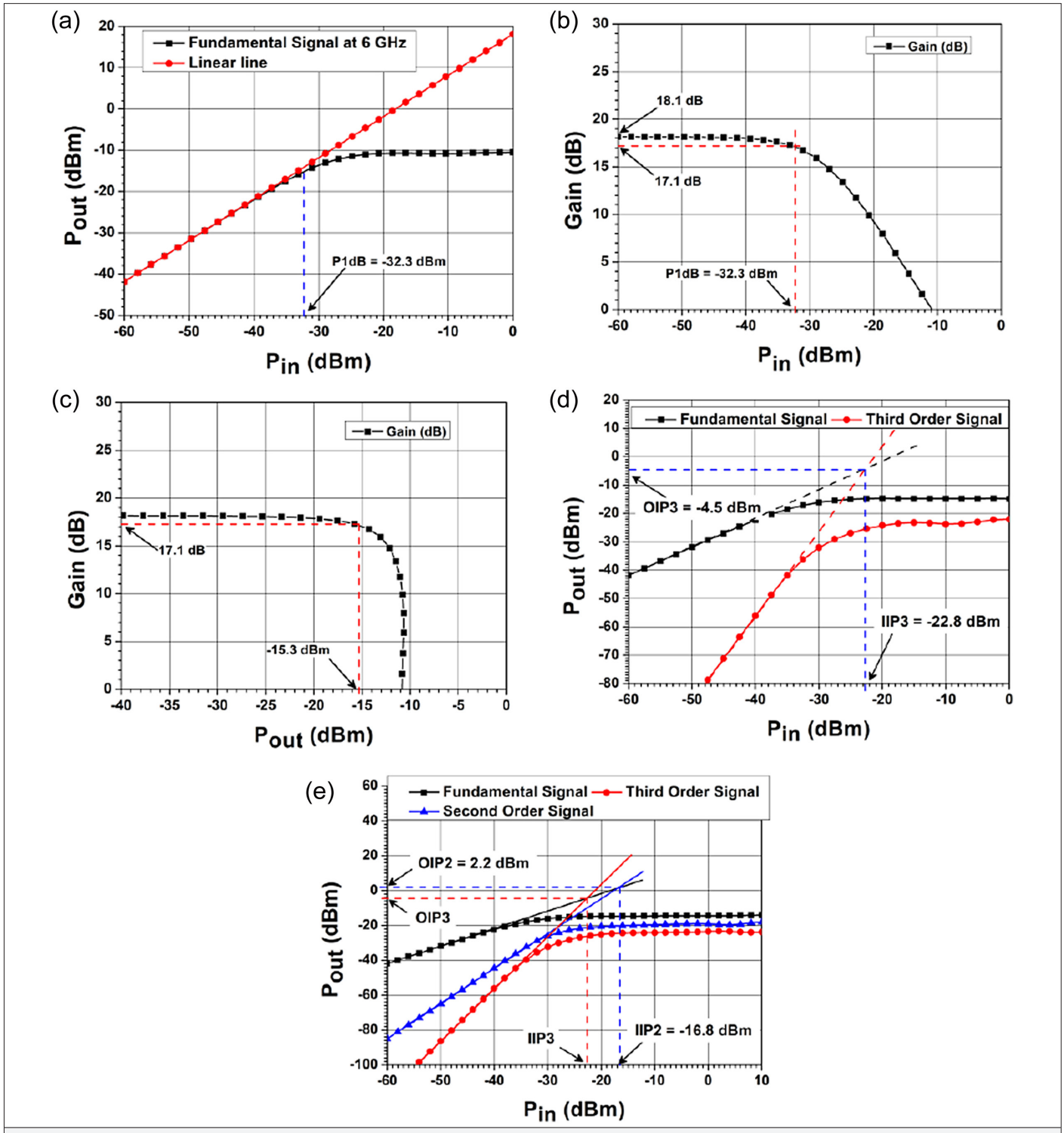

Fig. 16. Linearity performance: (a) 1-dB Compression, (b) Gain vs. input signal power, (c) gain vs. output signal power, (d) third-order intercept point (IIP_3), and (e) second-order intercept point (IIP_2).

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|} > 1 \quad (18)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (19)$$

The stability-factor plots for this LNA is shown in Fig. 18, and the value of K is much greater than 1 and $|\Delta|$ has a value less than 1 over the entire bandwidth.

The figure-of-merit (*FOM*) of the proposed LNA can be expressed by [16,20,23-25]

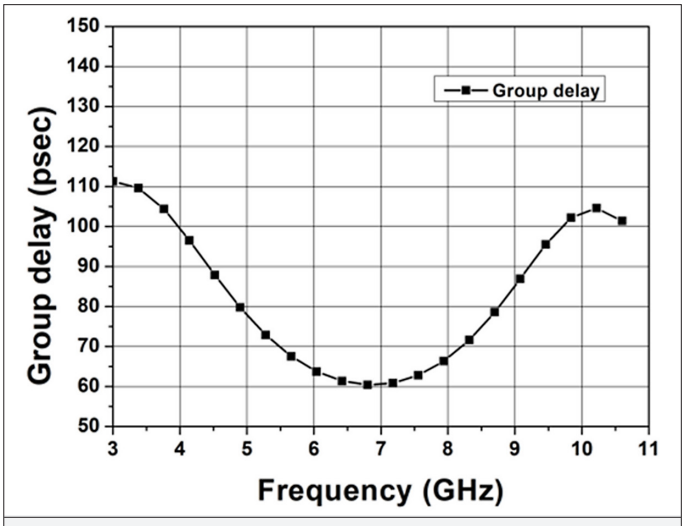

Fig. 17. Group-delay variation with frequency.

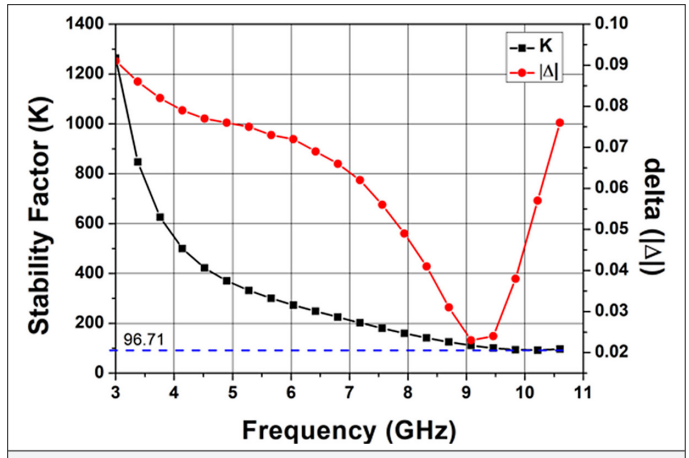

Fig. 18. Stability factor K and |Δ| for the proposed LNA.

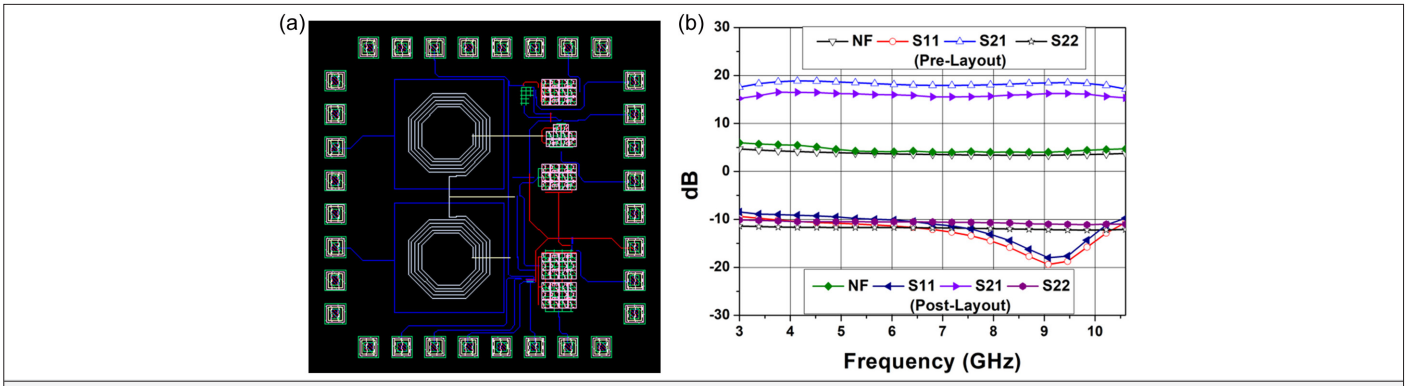

Fig. 19. (a) Layout of the proposed LNA; (b) pre- and post-layout NF, S_{11}, S_{21}, and S_{22} performance.

$$FOM[GHz/mW] = \frac{|S_{21}|_{abs} \times BW_{GHz}}{(F-1)\times P_{mW}} \quad (20)$$

where $|S_{21}|_{abs}$ and F are the absolute values of S_{21} and NF, respectively. The LNA has a very good *FOM* equal to 38.89.

Layout of the proposed low-noise amplifier with its post-layout simulation results are shown in Fig. 19. It has been depicted from the results that post-layout NF is varying from 3.99 to 5.7 dB, whereas S_{21} is varying from 15.21 dB at 3.0 GHz to 16.98 dB at 9.46 GHz. The input reflection coefficient (S_{11}) remains less than −8.452 dB, whereas output reflection coefficient (S_{22}) remains less than −10.13 dB. Table II presents the state-of-art and performance comparison with the existing works. It is depicted that the bandwidth of the inductor noise-canceling LNA proposed in [18] is only 0.1–1.4 GHz. Further, LNA proposed in this work consumes less power as compared to the LNAs proposed in [7,15,18,20,23,25]. Also NF of the LNA proposed in [16] is far greater than NF of the presented work, whereas it is comparable to the NF of LNAs proposed in [7,13,24]. The *IIP3* of the proposed LNA is low but is still acceptable and comparable with the LNA proposed in [16]. It highlights the fact that the proposed AI-based LNA exhibits high S_{21} while dissipating very less power.

IV. CONCLUSION

This paper presents a CG LNA design using the g_m-boosting technique. The main contribution of this paper is its active inductor-based input matching technique for UWB LNA design utilizing only two inductors that will benefits in terms of reduced chip area. Proposed LNA consists of g_m-boosting common gate stage, gain stage, and output buffer stage. G_m-boosting technique has been used to obtain high gain and dissipate less power as it decouples the existing trade-off between NF and input impedance. An active inductor was implemented for input impedance matching, thereby reducing the chip area. Proposed 90 nm CMOS LNA was designed using Cadence software. Proposed LNA demonstrates a flat power gain of 18 ± 0.8 dB, a minimum NF of 3.36 Db, and an input return loss less than −9.3 dB across the entire bandwidth. Proposed LNA circuit design operates in the frequency range of 3.1–10.6 GHz and dissipates 10.4 mW from 1.0 V supply. This makes the proposed LNA circuit suitable for most of the UWB wireless applications.

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TABLE II PERFORMANCE COMPARISON WITH THE EXISTING LITERATURES

Ref.	[18][S]	[7][S]	[23][S]	[13][S]	[25][PL]	[24][PL]	[15][S]	[16][S]	[20][S]	TW[S]
Year	2018	2021	2018	2012	2020	2019	2016	2015	2018	2021
Topology	Inductor less NC CCG	CCG with current reuse	CS-ID + NC	CG	CS-CG NC	CS-CD current-reuse	active g_m-boosted CG	CG	CS-ID with self-cascode current reused	CG-AI
Tech. (nm)	180	45	180	180	180	180	180	90	90	90
BW (GHz)	0.1–1.4	26–34	3–12	2.0–14	3–10.6	2–11	1~10.3	3.1–10.6	3.1–10.6	3.1–10.6
V_{dd} (V)	1.8	1.0	1.8	1.5	1	1	1.8	0.6	1	1
S_{21} (dB)	16.1 [max]	13.13[max]	19.24–20.24	9[avg]	12.1−13.4	12.35 ± 0.85	6	20.17 ± 0.39	20.10 ± 1.65	18.22[avg], 18.0 ± 0.8
S_{11} (dB)	<−10	<−9.58	<−10	<−10	<−10	<−10	<−10	<−10[@]	<−9	<−9.3
NF (dB)	2.8–3.4	3.08[min]	1.72–1.99	2.7–6.2	1.7–2.3	3.35 ± 0.8	4.1–4.7[EB]	1.11–1.41	1.2[a]	3.36–4.68
IIP_3 (dBm)	13–18.9	NA	−5.5	−3	−8	−3	11	−22	−4.22	−22.8
IIP_2 (dBm)	24–40	NA	NA	NA	NA	NA	NA	NA	NA	−16.8
Power (mW)	19	16	23.23	9	11.56	9.52	10.9	4.33	11.52	10.4
***FOM*(GHz/mW)**	NA	25.72[dB]	7.1	5.7	8.38	4.96	44[@@]	4.66[##], 89.2[&&&]	1.88 [##], 17.69[&&]	38.89

[##] $FOM = \frac{S_{21}(dB)}{P_{mW}}$; [&&] $FOM = \frac{S_{21,max}(dB) \times BW_{GHz}}{(F-1) \times P_{mW}}$; [&&&] $FOM = \frac{S_{21,max}(dB)}{(F-1) \times P_{mW}}$; [@@] $FOM = \frac{|S_{21}|_{abs} \times BW_{GHz} \times IIP3_{mW}}{(F-1) \times P_{mW}}$

[S]Simulation results; [PL]post-layout simulation results; CS, common source; ID, inductive degeneration; CG, common gate; NC, noise cancelling; CCG, complementary common gate.
[a]NFmin ; [avg]average; [max]maximum; [@]for 3.1–9.7 GHz; [EB]Excluding buffer; [min]minimum; [dB]FOM in dB.

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Humirah Majeed received her bachelor in technology in Electronics and Communication Engineering from Islamic University of Science and Technology, Awantipora Kashmir Jammu and Kashmir (India) in 2016 and Masters in technology from Shri Mata Vaishno Devi University, Katra Jammu and Kashmir (India) in 2019. Her research interests include RF integrated circuits and low power CMOS design.

Dr. Vikram Singh is working as an Assistant Professor in Shri Mata Vaishno Devi University, Katra Jammu & Kashmir, India. He has more than 13 years of experience in teaching and research. He did his Bachelor in Engineering from Kurukshetra University in 2004 and Masters of technology and PhD from Guru Jambheshwar University of Science & Technology in 2008 and 2019 respectively. He has published 15 research papers in International/National journals and conferences. His research interests include low power CMOS design, RF integrated circuit. He is a Life membership of ISTE, member of IETE (India), member of ISTE (India) and member of CSI (India).