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A New Simulated Grounded Inductor with Two-Terminal Active Devices

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ABSTRACT

In this study, a new simulated grounded inductor (SGI) is developed. It has a simple structure because it employs two-terminal active devices (TTADs). Moreover, it has a minimum number of passive elements, considering the TTAD-based configurations. However, there is a single passive element-matching constraint for two resistors. Derived from the developed SGI, a second-order voltage-mode universal filter application is given. With proper connection of inputs, it yields band-pass (BP), high-pass (HP), low-pass (LP), all-pass (AP), and notch filter (NF) responses. The performance of the developed circuits is verified through the SPICE simulation program. Additionally, an experimental test result is given for the developed SGI.

Index Terms—Current follower, negative impedance converter, simulated inductor, two-terminal active device, universal filter

I. INTRODUCTION

Analog circuit designers widely prefer the two-terminal active devices (TTADs) in many electronic circuit configurations because of advantages such as high performance and simplicity [1]. The TTADs, for instance, voltage followers (VFs), current followers (CFs), and negative impedance converters (NICs) are current-mode (CM) active devices; thus, they possess some advantages such as good bandwidth, high speed, and high accuracy [2]. A second-generation current conveyor (CCII) is a CM active device which can be used in the implementation of the TTADs.

Simulated inductors (SIs) [1,3-25] are significant elements in many electronic circuits, such as many filters, phase shifters, oscillators, etc. TTAD-based SIs have a simple structure [20]. Some SIs [1,18-25] are only TTAD-based configurations. The SIs in [1,20-23] include more than two unity gain cells. Several SIs [3-17] employ active building blocks (ABBs) with more than two terminals. Several SIs [1,3,15,20-23] use three or more ABBs. The SIs in [11,15,17,20,22] have a large number of transistors. A number of SIs [3,15,19,20,24] are composed of four or more passive components. The SIs in [4,13,14,21,24,25] are of the lossy inductor type. Some SIs [13,14,23] are negative type one. The SIs in [6-8,10,12] include Operational Transconductance Amplifier (OTAs); therefore they show limited high-frequency performance [26].

A new simulated grounded inductor (SGI) comprising two TTADs is developed in this paper. It contains only one capacitor and two resistors. However, there is a single passive element-matching constraint for the two resistors. As an application example, a second-order voltage-mode (VM) universal filter configuration is given. It can provide band-pass (BP), high-pass (HP), low-pass (LP), notch filter (NF), and all-pass (AP) responses. The performance of the developed circuits is validated via the SPICE simulations by using 0.18 µm CMOS technology parameters. Additionally, an experimental test is achieved for the developed SGI to endorse the theory.

This paper consists of the following sections:

Following this introduction, the circuit theory and the developed simulated inductor are introduced in Section II. Parasitic analysis of the simulated inductor is presented in Section III. The second-order universal filter application is given in Section IV. While the simulation results are offered in Section V, the experimental test result is presented in Section VI. Finally, the developed circuits are concluded in Section VII.

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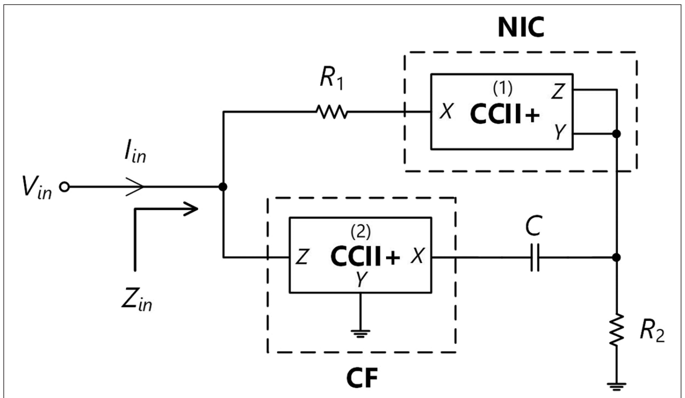

Fig. 1. The developed simulated inductor circuit diagram.

II. Circuit Description

The plus-type CCII (CCII+) is a three-terminal active device. If the chosen current directions are fed into the CCII+, the characteristic equation can be defined as follows:

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} \beta & 0 \\ 0 & 0 \\ 0 & \alpha \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \end{bmatrix} \tag{1}$$

where α means nonideal current gain and β means nonideal voltage gain. The α and β gains are ideally equal to unity. The CCII+ is used to actualize NIC and VF elements. The internal structure of the CCII+, which has sixteen MOS transistors, is given in [27,28].

The developed SGI is shown in Fig. 1. It consists of an NIC, a CF, two resistors (one of them is grounded), and a capacitor. The NIC is realized by combining the *Y* and *Z* terminals of the CCII+. The CF is realized by grounding of the *Y* terminal of the CCII+.

As a result of the routine analysis of the developed SGI without nonideal gains, input impedance is obtained as follows:

$$Z_{in} = \frac{V_{in}}{I_{in}} = R_1 - R_2 + sCR_1R_2 \tag{2}$$

If $R_1 = R_2 = R$ is taken, (2) becomes

$$Z_{in} = \frac{V_{in}}{I_{in}} = sCR^2 = sL_{eq} \tag{3}$$

where $L_{eq} = CR^2$. If nonideal gains are considered, input impedance of the developed SGI is found as:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{CR_1R_2s + R_1 - \alpha_1\beta_1R_2}{(1-\alpha_1\alpha_2)CR_2s + 1} \tag{4}$$

III. Influence of the Parasitic Impedances

Parasitic impedances of the CCII+ are shown in Fig. 2. If current directions are chosen and fed into the CCII+, the equation with parasitic impedances can be given as

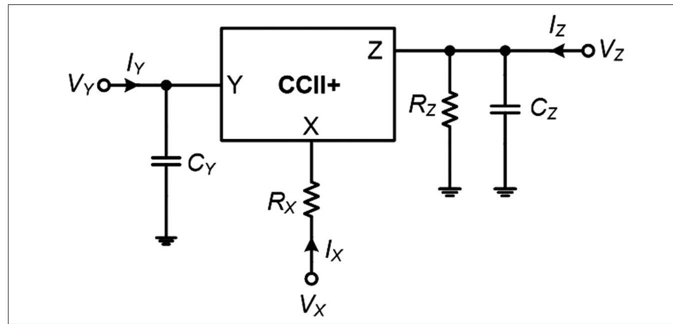

Fig. 2. CCII+ with parasitic impedances.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} sC_Y & 0 & 0 \\ 1 & R_X & 0 \\ 0 & 1 & sC_Z + \dfrac{1}{R_Z} \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{5}$$

After the routine analysis of the developed SGI without nonideal gains, input impedance is obtained as follows:

$$Z_{in}(s) = \frac{1}{sC_{Z2}} // R_{Z2} // Z_1 \tag{6}$$

where Z_1 can be given as

$$Z_1 = \left(R_1 + R_{X1} - \frac{R_2 // R_{Z1}}{1 + s\left(C_{Z1} + C_{Y1}\right)\left(R_2 // R_{Z1}\right)} + \frac{sC}{1 + sCR_{X2}} \cdot \frac{\left(R_1 + R_{X1}\right)\left(R_2 // R_{Z1}\right)}{1 + s\left(C_{Z1} + C_{Y1}\right)\left(R_2 // R_{Z1}\right)} \right) \tag{7}$$

IV. SECOND-ORDER VOLTAGE-MODE UNIVERSAL FILTER APPLICATION

As an application of the developed SGI, a second-order voltage-mode (VM) universal filter application is given in Fig. 3. It includes an NIC, a CF, three resistors (one of them is grounded), and two

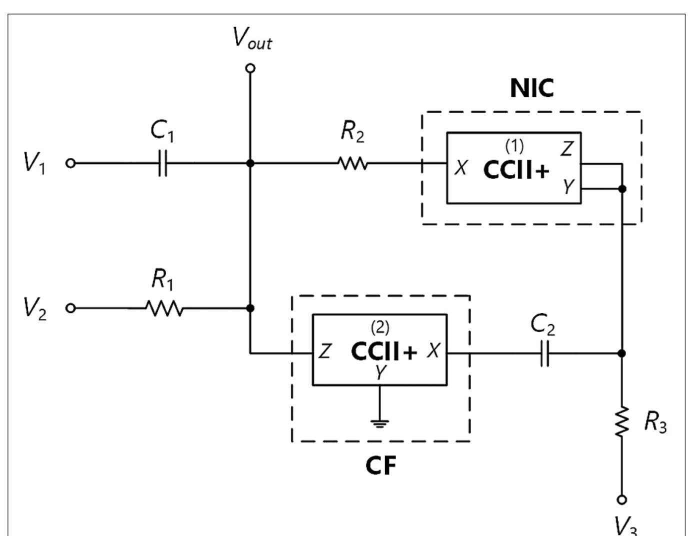

Fig. 3. Circuit diagram of the universal filter application.

capacitors. The output voltage of the second-order VM universal filter application is evaluated as:

$$V_{out}=\frac{C_1C_2R_1R_2R_3V_1s^2+((R_2-R_3)C_1R_1V_1+(R_3V_2-R_1V_3)C_2R_2)s+(R_2-R_3)V_2+R_1V_3}{C_1C_2R_1R_2R_3s^2+(C_2R_2R_3+(R_2-R_3)C_1R_1)s+R_1+R_2-R_3} \quad (8)$$

One observes from (8) that the following conditions should be met for stability [29]:

$$C_2R_2R_3+\left(R_2-R_3\right)C_1R_1>0 \quad (9a)$$

$$R_1+R_2-R_3>0 \quad (9b)$$

If $R_1 = R_2 = R_3 = R$ is considered, (8) becomes

$$V_{out}=\frac{C_1C_2R^2V_1s^2+C_2R(V_2-V_3)s+V_3}{C_1C_2R^2s^2+C_2Rs+1} \quad (10)$$

From (10), the following filter functions are obtained with proper connection of inputs:

- LP: if V_2 and V_3 are taken as input and $V_1 = 0$.
- BP: if V_2 is taken as input and $V_1 = V_3 = 0$.
- HP: if V_1 is taken as input and $V_2 = V_3 = 0$.
- AP: if V_1 and V_3 are taken as input and $V_2 = 0$.
- NF: if V_1, V_2, and V_3 are taken as input.

The angular resonant frequency (ω_0) and the quality factor (Q) are, respectively, calculated by:

$$\omega_0=\frac{1}{R\sqrt{C_1C_2}} \quad (11a)$$

$$Q=\sqrt{\frac{C_1}{C_2}} \quad (11b)$$

The passive element sensitivities are calculated as below:

$$S_R^{\omega_0}=-1\ ;\ \ S_{C_1}^{\omega_0}=S_{C_2}^{\omega_0}=S_{C_2}^{Q}=-S_{C_1}^{Q}=-\frac{1}{2}$$

The angular resonant frequency (ω_0) and the quality factor (Q), without considering any matching conditions, are respectively calculated by:

$$\omega_0=\sqrt{\frac{R_1+R_2-R_3}{C_1C_2R_1R_2R_3}} \quad (12a)$$

$$Q=\frac{\sqrt{C_1C_2R_1R_2R_3\left(R_1+R_2-R_3\right)}}{C_1R_1(R_2-R_3)+C_2R_2R_3} \quad (12b)$$

The passive element sensitivities, without considering any matching conditions, are obtained as:

$$S_{R_1}^{\omega_0}=-\frac{R_2-R_3}{2(R_1+R_2-R_3)}\ ;\ S_{R_2}^{\omega_0}=-\frac{R_1-R_3}{2(R_1+R_2-R_3)}\ ;\ S_{R_3}^{\omega_0}=-\frac{R_1+R_2}{2(R_1+R_2-R_3)}\ ;$$

$$S_{C_1}^{\omega_0}=S_{C_2}^{\omega_0}=-\frac{1}{2}\quad S_{R_1}^{Q}=-\frac{C_2R_2R_3\left(2R_1+R_2-R_3\right)-C_1R_1\left(R_2-R_3\right)^2}{2\left(R_1+R_2-R_3\right)\left(C_1R_1\left(R_2-R_3\right)+C_2R_2R_3\right)}$$

$$S_{R_2}^{Q}=-\frac{C_2R_2R_3\left(R_1-R_3\right)+C_1R_1\left(R_1R_2+R_1R_3+R_2R_3-R_3^2\right)}{2\left(R_1+R_2-R_3\right)\left(C_1R_1\left(R_2-R_3\right)+C_2R_2R_3\right)}$$

$$S_{R_3}^{Q}=-\frac{C_2R_2R_3\left(R_1+R_2\right)-C_1R_1\left(R_1R_2+R_2^2+R_1R_3-R_2R_3\right)}{2\left(R_1+R_2-R_3\right)\left(C_1R_1\left(R_2-R_3\right)+C_2R_2R_3\right)}$$

$$S_{C_1}^{Q}=-\frac{C_2R_2R_3\left(-R_1-R_2+R_3\right)+C_1R_1\left(R_1R_2+R_2^2-R_1R_3-2R_2R_3+R_3^2\right)}{2\left(R_1+R_2-R_3\right)\left(C_1R_1\left(R_2-R_3\right)+C_2R_2R_3\right)}$$

$$S_{C_2}^{Q}=\frac{C_2R_2R_3\left(-R_1-R_2+R_3\right)+C_1R_1\left(R_1R_2+R_2^2-R_1R_3-2R_2R_3+R_3^2\right)}{2\left(R_1+R_2-R_3\right)\left(C_1R_1\left(R_2-R_3\right)+C_2R_2R_3\right)}$$

Considering nonideal gains and without considering any matching conditions, the output voltage in (8) respectively turns into:

$$V_{outn}=\frac{n_2s^2+n_1s+n_0}{d_2s^2+d_1s+d_0} \quad (13)$$

where

$$n_0=V_2(R_2-R_3\alpha_1\beta_1)+R_1\beta_1V_3 \quad (14a)$$

$$n_1=C_1R_1V_1(R_2-R_3\alpha_1\beta_1)+C_2R_2(R_3V_2-R_1V_3\alpha_2) \quad (14b)$$

$$n_2=C_1C_2R_1R_2R_3V_1 \quad (14c)$$

$$d_0=R_1+R_2-R_3\alpha_1\beta_1 \quad (14d)$$

$$d_1=C_1R_1(R_2-R_3\alpha_1\beta_1)+C_2R_3(R_1+R_2-R_1\alpha_1\alpha_2) \quad (14e)$$

$$d_2=C_1C_2R_1R_2R_3 \quad (14f)$$

From (13) and (14), ω_0 and Q with nonideal gains are respectively found as:

$$\omega_{0n}=\sqrt{\frac{R_1+R_2-R_3\alpha_1\beta_1}{C_1C_2R_1R_2R_3}} \quad (15a)$$

$$Q_n=\frac{\sqrt{C_1C_2R_1R_2R_3(R_1+R_2-R_3\alpha_1\beta_1)}}{C_1R_1(R_2-R_3\alpha_1\beta_1)+C_2R_3(R_1+R_2-R_1\alpha_1\alpha_2)} \quad (15b)$$

V. SIMULATION RESULTS

The developed SGI and its filter application are simulated in the PSPICE AD 17.4 (Cadence Design Systems, CA, USA) program by using TSMC 0.18 µm CMOS technology parameters as given in [30]. The *W/L* ratios of the MOS transistors in simulations are listed in Table I. The symmetrical power supply voltages are selected as ±1.25 V. The passive component values of the SGI in Fig. 1 are determined as $C = 100$ pF and $R_1 = R_2 = 3$ kΩ; therefore, $L_{eq} = 0.9$ mH is obtained. Parasitic impedances of the CCII+ used in simulations are calculated as $R_X \cong$ 126 mΩ, $R_Z \cong$ 31 kΩ, $C_Z \cong$ 45.5 fF and $C_Y \cong$ 37 fF.

The magnitude and phase responses of the developed SGI are shown in Fig. 4. The simulated and ideal magnitude responses overlap in the frequency range of 100 kHz–10 MHz while the simulated phase response approximates the ideal ones in the same frequency range.

TABLE I. *W/L* RATIOS OF THE MOS TRANSISTORS

Transistor	Type	*W/L* (μm)
M_1, M_2, M_3, M_7, M_8	PMOS	39/0.5
M_4, M_5	PMOS	65/0.5
M_6, M_9, M_{14}, M_{15}, M_{16}	NMOS	13/0.5
M_{10}	NMOS	52/0.5
M_{11}	PMOS	156/0.5
M_{12}, M_{13}	NMOS	19.5/0.5

A sinusoidal input current signal with a 100 μA peak at 500 kHz is applied to input of the developed SGI. The input current, simulated, and ideal output voltage signals are shown in Fig. 5. It is seen that the simulated and ideal voltage outputs are compatible with each other. A triangular current signal with a 100 μA-peak at 500 kHz is applied to input of the developed SGI. The simulated and ideal output voltage signals shown in Fig. 6 are obtained as a square signal waveform.

A Monte Carlo (MC) analysis with 300 runs is performed with 10% variation of the capacitor value using uniform distribution. The magnitude and phase responses of the developed SGI are drawn in Fig. 7.

Sinusoidal input currents between 0 and 140 μA at 500 kHz are applied. Hence, total harmonic distortion (THD) variations of the developed SGI are drawn in Fig. 8.

For the VM universal filter application, the passive elements are selected as $R_1=R_2=R_3=3$ kΩ and $C_1=C_2=100$ pF; therefore, $f_0=530.5$ kHz and $Q=1$ are ideally found. The HP and LP filter gain responses are drawn in Fig. 9. The AP and NF gain and phase responses are respectively drawn in Fig. 10 and 11. All the ideal responses are close to the simulated ones.

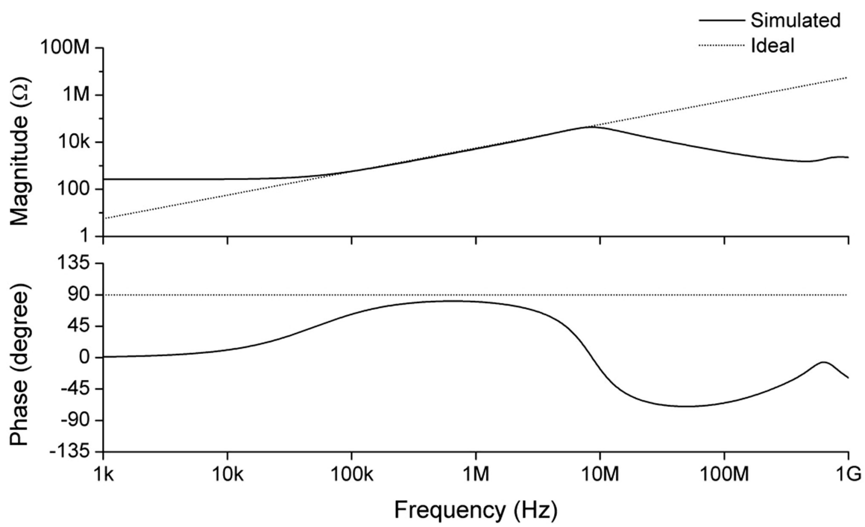

Fig. 4. Magnitude and phase responses of the developed simulated grounded inductor.

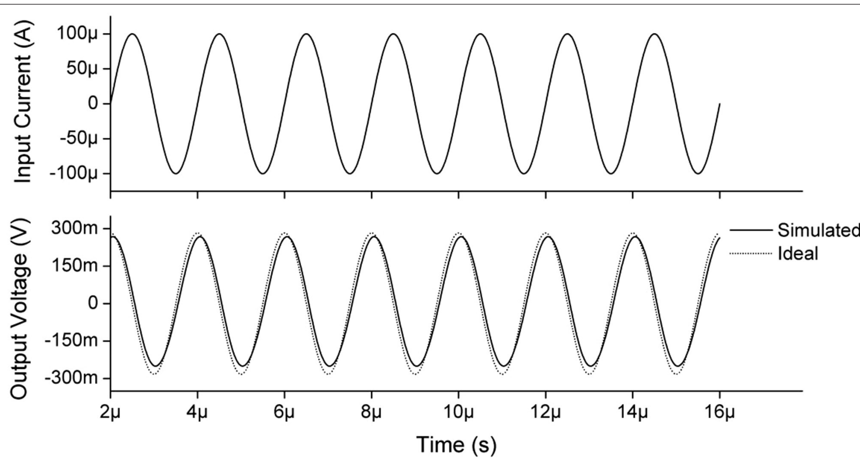

Fig. 5. The sinusoidal signal response of the developed simulated grounded inductor.

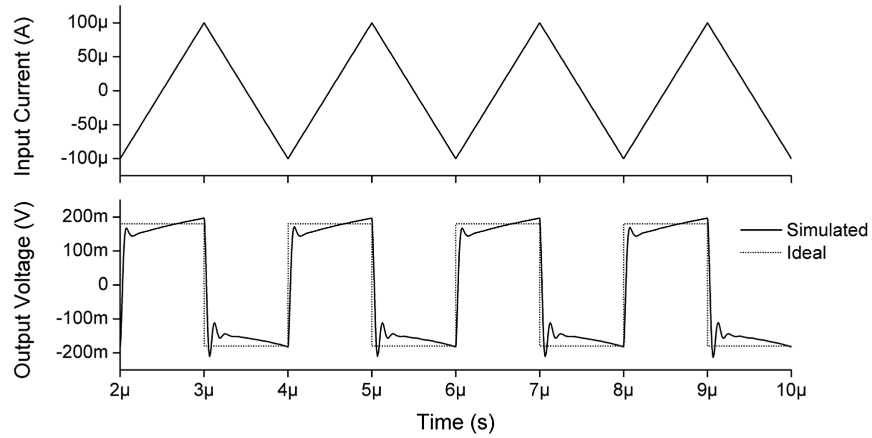

Fig. 6. The triangular signal response of the developed simulated grounded inductor.

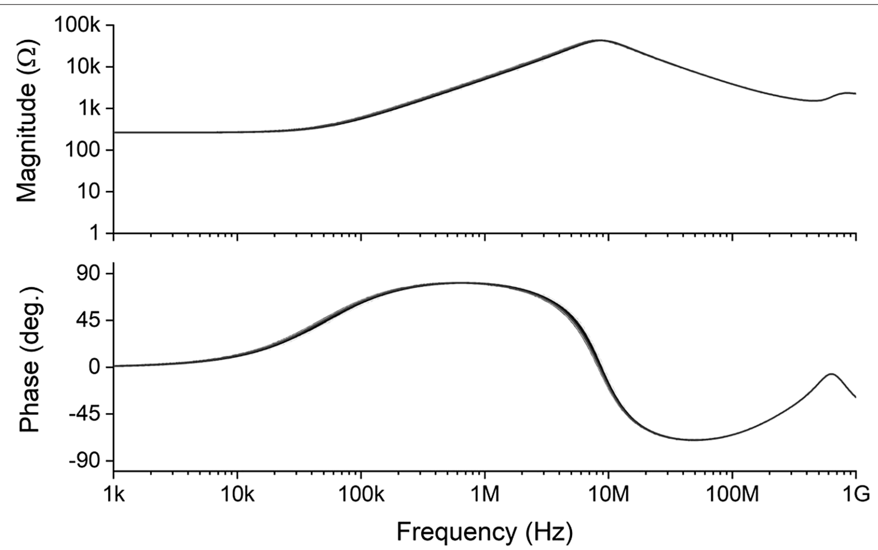

Fig. 7. Monte Carlo analysis of the developed SGI with 10% change of the capacitor value.

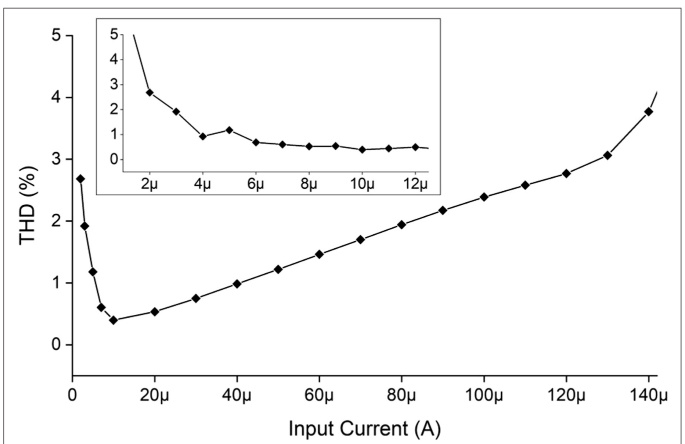

Fig. 8. THD variation of the developed simulated grounded inductor.

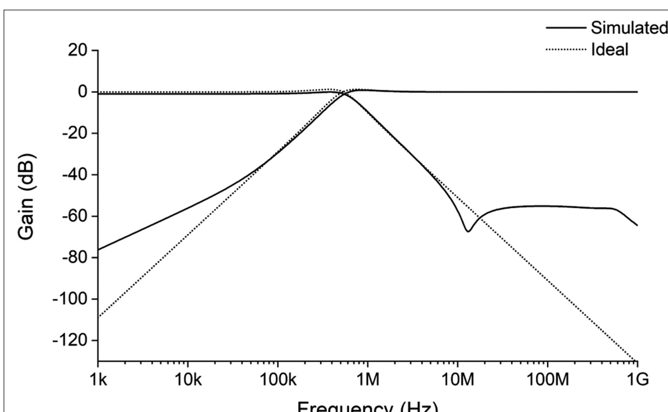

Fig. 9. High-pass and low-pass filter gain responses.

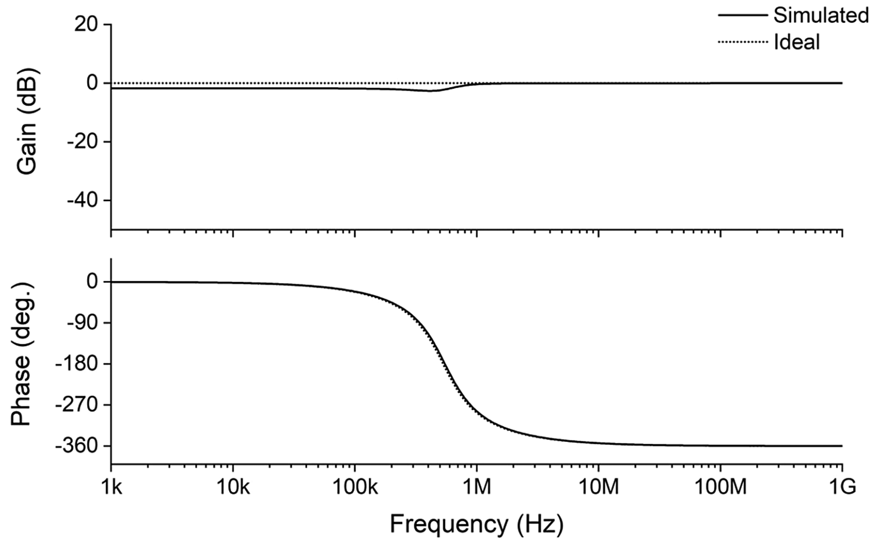

Fig. 10. All-pass filter gain and phase responses.

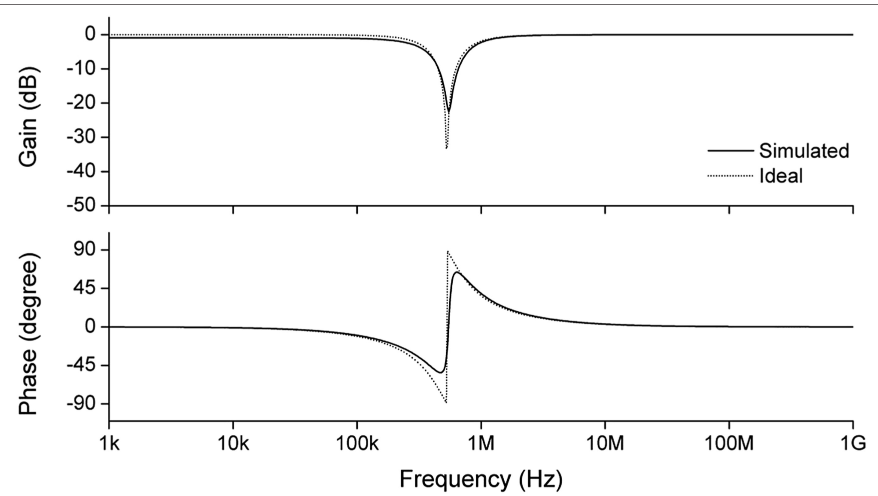

Fig. 11. Notch filter gain and phase responses.

For the BP filter, an MC analysis with 300 runs is performed with 10% uniform change of the capacitor values. While changing the capacitor values, the gain response of the BP filter is shown in Fig. 12. Similarly, an MC analysis with 300 runs is performed with a 2% uniform change of the resistor values for the BP filter. While changing the resistor values, the gain response of the BP filter is shown in Fig. 13. The gain responses of the BP filter shown in Fig. 12 and 13 are compatible with Fig. 9.

The total power consumptions of the developed SGI and its filter application are respectively found as 4.62 mW and 4.30 mW. Some TTAD-based SIs in related literature are summarized in Table II.

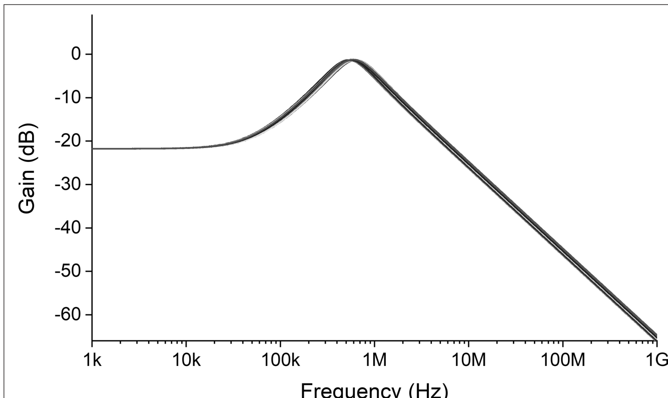

Fig. 12. Monte Carlo analysis of the BP filter responses with 10% change of the capacitor values.

VI. An Experimental Test Result

An experimental test is performed to show input/output characteristics of the developed SGI. The NIC and CF can be realized by using commercially available integrated circuit devices such as

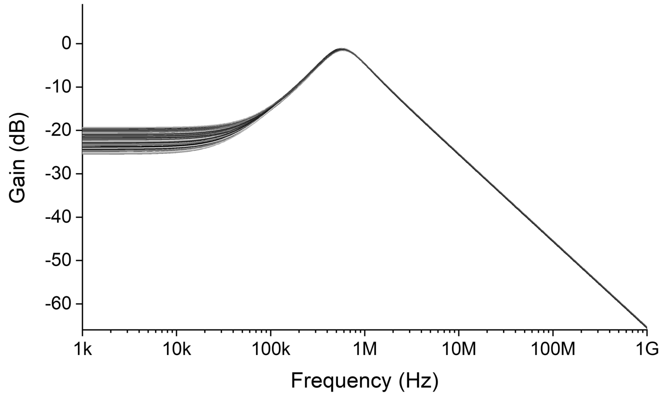

Fig. 13. Monte Carlo analysis of the BP filter responses with 2% change of the resistor values.

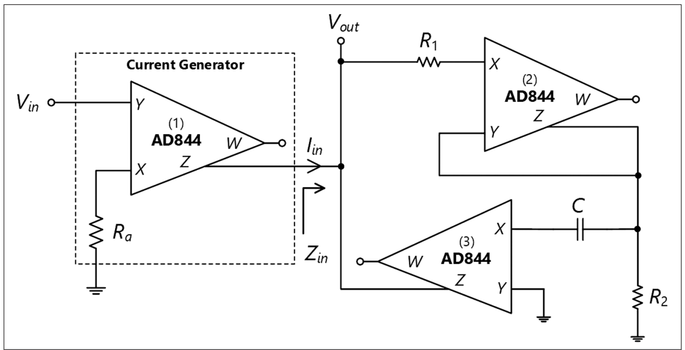

Fig. 14. Experimental test circuit with AD844s.

TABLE II. THE COMPARISON TABLE FOR SOME TTAD-BASED SIS

Ref. No.	Number of Transistors	Number of ABBs	Number of Passive Components R	Number of Passive Components C	Type	Grounded/ Floating SI	Power Dissipation	Technology	Power Supply (V)
[1]	27	2 VFs, 1 CF	2*	1	Lossless	Grounded	-	0.13 μm	±0.75
[18]	36	1 INIC, 1 VNIC	2	1	Lossless	Grounded	5.32 mW	0.13 μm	±0.75
[19]	-	2 NICs	3	1	Lossless	Grounded/Floating	-	-	-
[20]	80	2 INICs, 2 CFs, 1 VF	4	1	Lossless	Floating	-	0.25 μm	±1.25
[21]	30	2 VFs, 1 CF	2*	1	Lossy	Grounded	6.87 mW	0.25 μm	±1.25
[22]	52	2 VFs, 2 CFs	2	1	Lossless	Grounded	-	0.5 μm	±1.5
[23]	-	1 VF, 2 CFs	1	2	Negative	Grounded	-	AD844	±12
[24]	32	1 NIC	2	2	Lossy	Grounded	1.36 mW	0.35 μm	±1.5
[25]	-	2 INICs	2	1	Lossy	Floating	-	AD844	±12
This work	32	1 INIC, 1 CF	2	1	Lossless	Grounded	4.62 mW	0.18 μm	±1.25

*Intrinsic resistor, - not specified. INIC: Current NIC; VNIC: Voltage NIC.

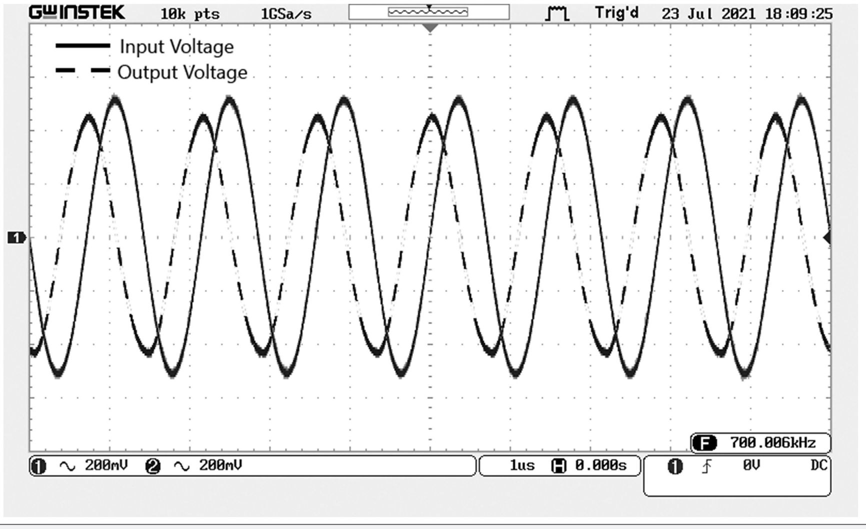

Fig. 15. Input and output voltage signals of the developed simulated grounded inductor in experiment.

AD844s (Analog Devices, MA, USA) [18]. Input voltage is chosen as 500 mV-peak at 700 kHz. The first AD844 is used for the input of the developed SGI to generate input current. The passive elements are selected as $R_a = 5.6$ kΩ, $R_1 = R_2 = 3$ kΩ and $C = 100$ pF. Therefore, a sinusoidal input current with 90 μA at approximately 700 kHz is applied to input of the SGI. Symmetrical power supplies are chosen as ±6 V. The schematic of the experimental test circuit is given in Fig. 14. The input and output (I/O) voltage signals in the experiments are given in Fig. 15. It is seen that phase difference between I/O voltage signals is about −90°; therefore the SI current/voltage characteristics are provided.

VII. CONCLUSION

A new SGI employing two TTADs is developed in this paper. It contains a minimum number of passive elements considering TTAD-based configurations, but it has a single passive element-matching constraint for two resistors. A second-order VM universal filter is given as an application example, which can provide LP, BP, HP, AP, and NF responses with proper connection of inputs. Several SPICE simulations and an experimental test result are presented to show the performance of the developed circuits. The experimental and simulation results are close to the ideal ones.

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