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Improved Interleaved DC-DC Converter Without Auxiliary Switches: Analysis and Experimental Validation

Veera Venkata Subrahmanya Kumar Bhajana[1], Pravat Biswal[1], Pavel Drabek[2], Vijay Kakani[3]

[1]School of Electronics Engineering, KIIT University, Bhubaneswar, India
[2]Regional Innovation Centre for Electrical Engineering, University of West Bohemia, Plzeň, Czech Republic
[3]Department of Integrated System Engineering, Inha University, Incheon, South Korea

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WHAT IS ALREADY KNOWN ON THIS TOPIC?

- Interleaved DC-DC converters are well-known in power electronics for their ability to reduce input/output current ripple, distribute thermal stress, and enhance power conversion efficiency. These converters operate by paralleling multiple phases (usually identical converters) with interleaved switching to smooth the overall system response and reduce passive component size.

Corresponding Author:
Veera Venkata Subrahmanya Kumar Bhajana

E-mail:
bvvs.kumarfet@kiit.ac.in, bvvskumar@ieee.org

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ABSTRACT

This paper presents a new two-phase interleaved boost converter for photovoltaic applications. An interleaved boost converter improved with an additional resonant circuit is proposed. The auxiliary circuit with a resonant inductor, a capacitor, and two diodes is used to obtain a zero-voltage switching condition. This converter has the advantages of reduced switching losses, better efficiency, and reduced input current ripples. The operating principles and design analysis are also presented. To validate the theoretical analysis, a prototype of a 48 V/260 V/200 W converter system is developed, and an efficiency of 96% is obtained.

***Index Terms*—**Interleaved boost converter, soft-switching, zero voltage switching (ZVS), zero current switching (ZCS)

I. INTRODUCTION

Nowadays, boost converters are widely employed in power electronic systems to step up low input voltages to higher, regulated output voltages. These converters play a critical role in applications that utilize renewable and distributed energy sources, including photovoltaic (PV) systems, Direct Current (DC) microgrids, and battery storage systems [1]–[4]. Their ability to efficiently interface low-voltage energy sources with high-voltage loads or distribution networks makes them indispensable in modern power conversion architectures. To reduce input current and output voltage ripples, conventional boost converters have been enhanced into an interleaved boost converter (IBC) configuration. These IBCs not only provide improved ripple performance but also facilitate higher efficiency and better voltage regulation. To achieve optimal performance, various control strategies such as maximum power point tracking [5], [6] and adaptive feedback control techniques [7] have been integrated into IBC designs. To minimize input current ripples, an interleaved converter incorporating auxiliary switches in addition to the main switches was proposed in [8]. Though effective, this topology requires a greater number of auxiliary components, making it more suitable for low-voltage applications. In another approach, a dual coupled-inductor (CI)-based interleaved boost converter with an integrated clamping capacitor was introduced in [9] to enhance efficiency by reducing voltage stress on the switches. However, this configuration is primarily applicable to low-power scenarios due to its limited scalability. Furthermore, to obtain a soft-switching condition in an interleaved boost converter [10], a coupled inductor and clamping capacitors are incorporated. An IBC is assisted by a single auxiliary circuit, either without CIs [11] or with CIs [12-15], and achieves soft-switching conditions at low power levels. Although a zero-voltage transition (ZVT) condition is obtained by operating the auxiliary switch frequency at a higher frequency than the main switching frequency, this also leads to increased additional current stresses. Furthermore, the use of CIs, an increased number of switched capacitor cells, and auxiliary circuits in IBCs [16] helps enhance voltage gain and enables soft-switching. To improve switching performance and reduce losses, soft-switching techniques have been incorporated into IBC designs. One such approach modifies

WHAT THIS STUDY ADDS ON THIS TOPIC?

- This study introduces a novel interleaved DC-DC converter topology that achieves soft-switching operation and high efficiency without the need for auxiliary switches, which are commonly used in traditional designs to facilitate zero-voltage or zero-current switching. By integrating resonant elements directly into the main power path of the interleaved structure, the proposed converter achieves zero-voltage switching (ZVS) of the primary power switches. This significantly minimizes switching losses and electromagnetic interference (EMI), thereby improving overall system efficiency.

the conventional IBC topology by introducing a large inductor and integrating snubber capacitors, thereby obtaining ZVT operation and reducing switching losses [17]. Alternatively, another ZVT-based IBC design employs a large inductor in conjunction with an auxiliary switch to achieve the desired soft-switching condition [18]. Despite their advantages, these converters are primarily constrained to low-voltage and low-power applications due to their increased complexity and limited scalability. Additionally, soft-switching in an IBC can be achieved through the integration of an auxiliary circuit [19], while the incorporation of voltage multiplier cells further enhances the voltage gain. However, this converter operates at lower power levels, which facilitates the realization of the ZVT condition and contributes to an overall improvement in voltage gain. To further increase the overall gain, the number of windings in the CIs is increased. Additional passive lossless clamp circuits [20] and active clamp circuits [21] are employed to recycle leakage energy, enabling operation at high output power. In another approach, increasing the turns ratio of CIs improves voltage gain, and zero-current switching (ZCS) is achieved using a lossless clamping circuit (LCC) in the IBC [22]. This configuration reduces turn-off losses and further boosts overall gain. Additionally, another IBC with LCCs [23-25] achieves zero-voltage switching (ZVS) during turn-off, while retaining all the aforementioned benefits. A two-phase soft-switching interleaved boost converter [26] is implemented with auxiliary switches, pulse transformers, and resonant capacitors. The auxiliary circuit is incorporated to achieve zero-voltage and zero-current switching for the main switches. However, this results in a bulkier converter with increased control complexity. To enhance the voltage conversion ratio in an interleaved boost converter [27], a magnetically coupled cell with a voltage multiplier is employed, along with two snubber cells to achieve ZVS during turn-on. However, the addition of auxiliary snubber cells significantly increases the total device count, thereby escalating both the volume and cost. Similarly, an interleaved boost converter without a voltage multiplier cell was implemented using only resonant circuits to achieve soft-switching operation [28]. However, this converter achieves high efficiency only at a nominal conversion gain. To reduce input current ripples, enhance stability, and improve transient response, various control strategies have been developed for interleaved converters, including the Type-III controller [29], sliding mode control [30], and model predictive current control [31]. The existing converters exhibit the following drawbacks.

- More number of passive components
- More number of active components
- Electromagnetic interference (EMI)
- Increased control complexity
- Operation at low output power

Fig. 1 illustrates the overall configuration of an interleaved boost converter integrated with renewable energy sources, supplying power to loads like DC microgrids and electric vehicles (EVs). The voltage from low-voltage sources, such as photovoltaic cells, is typically from 12 V to

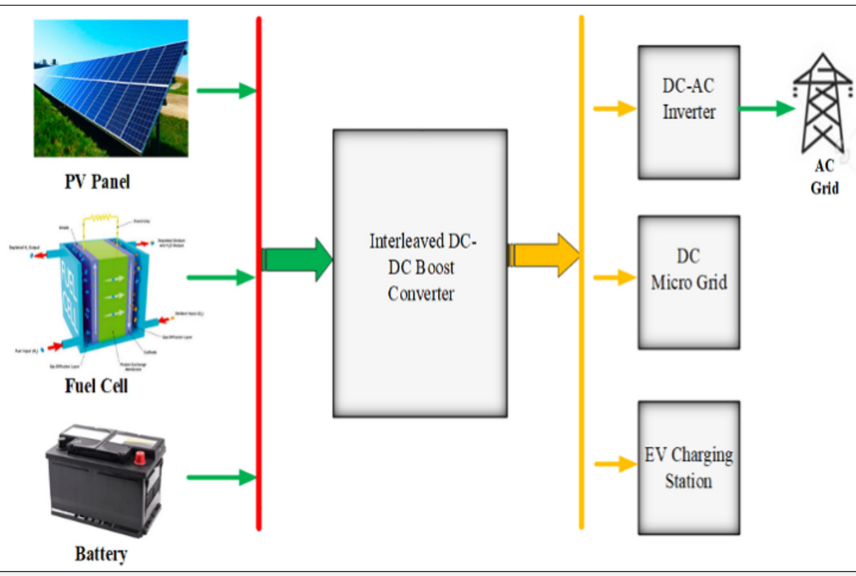

Fig. 1. Generalized structure of renewable energy sources with an interleaved boost converter.

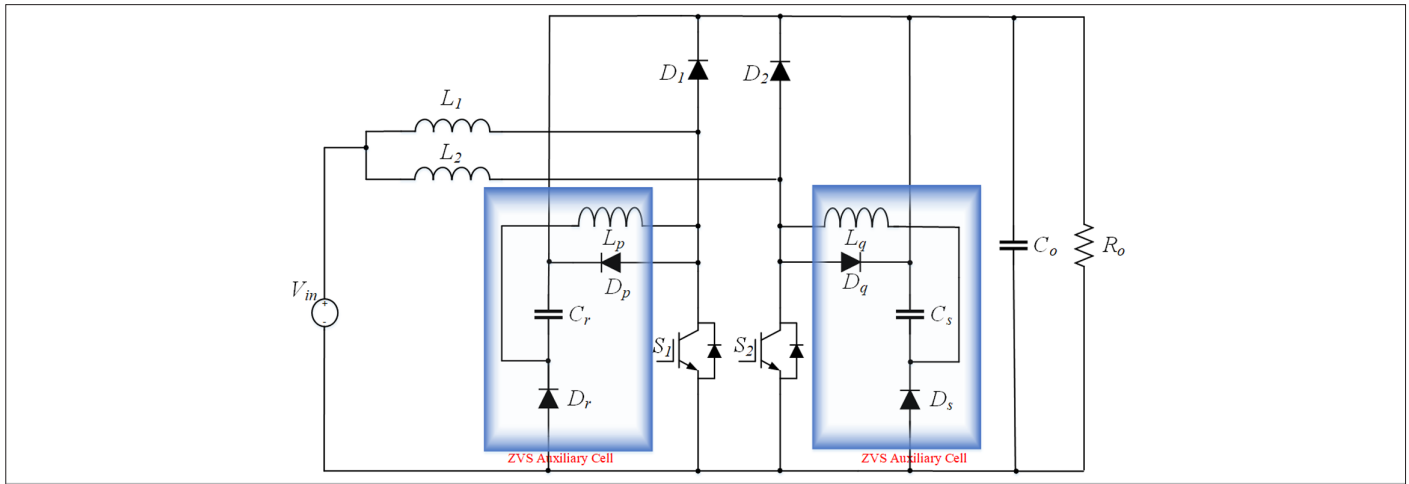

Fig. 2. Proposed interleaved boost converter with dual auxiliary cells.

48 V, while the IBC delivers a desirable voltage between 200 V and 500 V to the load.

To overcome the aforementioned limitations, this paper proposes a new soft-switching interleaved boost converter that incorporates simple active-passive cells, consisting of a diode, a resonant capacitor, and a resonant inductor. The proposed converter offers the following significant merits over existing IBCs:

- Fewer active and passive components
- Capable of operating at higher power levels
- Reduced switching losses
- Lower voltage stresses on the switching devices

This paper is organized as follows: Section II discusses the circuit description and operating principles; Section III presents the design analysis; Section IV covers the loss analysis; Section V presents the simulation results; and Section VI provides the experimental verification.

II. DESCRIPTION AND OPERATING MODES

A. Description of Proposed Interleaved Boost Converter

Fig. 2 illustrates the proposed IBC without auxiliary switches. The conventional IBC is enhanced by adding two auxiliary circuits to each leg of the converter. The conventional IBC consists of the main switching devices S1 and S2, two input inductors L_1 and L_2, and two diodes D_1 and D_2. The primary leg is supported by an auxiliary circuit that includes a resonant inductor (L_p), a resonant capacitor (C_r), and two diodes (D_p and D_r). Similarly, the secondary leg is assisted by an auxiliary circuit containing a resonant inductor (L_q), a resonant capacitor (C_s), and two diodes (D_q and D_s). The operation of the proposed converter, depicted in the key waveform in Fig. 3, is divided into nine intervals (t_0 to t_9). The corresponding equivalent circuits for each interval are shown in Fig. 4–11. Prior to the operation analysis on the Soft-Switched Interleaved Boost Converter, the following assumptions are made:

(1) All IGBTs and passive elements are considered to be ideal.
(2) The parasitic elements in the circuit are ignored.
(3) The filter capacitor (C_o) is sufficiently large to ignore output voltage ripples.
(4) Inductors L_1 and L_2 have large inductance, and their currents are assumed to be constant.

B. Operating Modes

Interval-1 (t_0-t_1): At t_0, the voltage across S_1 is zero, and the body diode of S_1 starts conducting, and the current through L_p changes its

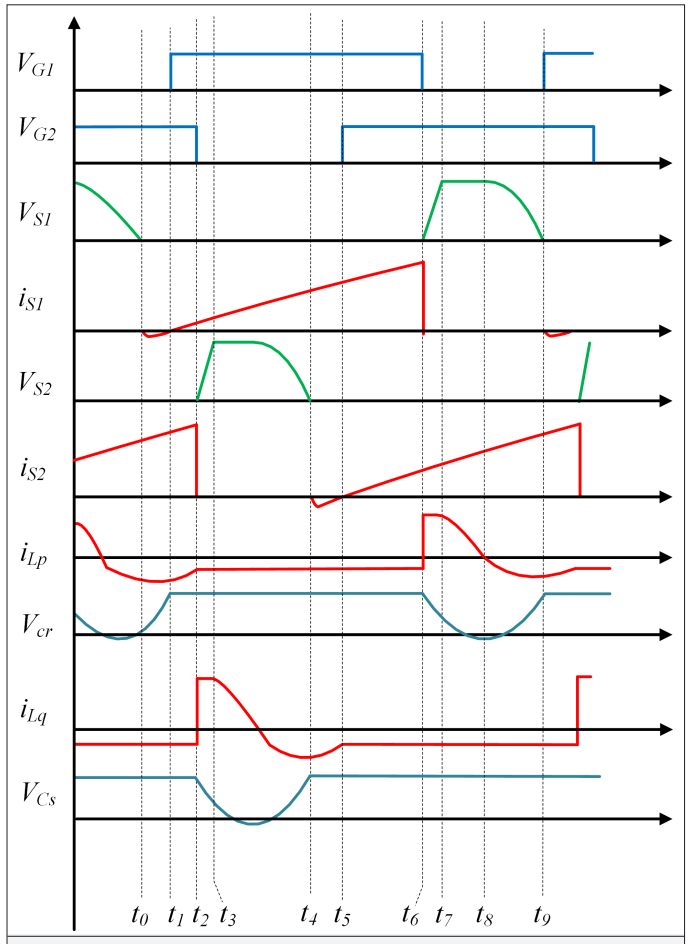

Fig. 3. Key waveforms.

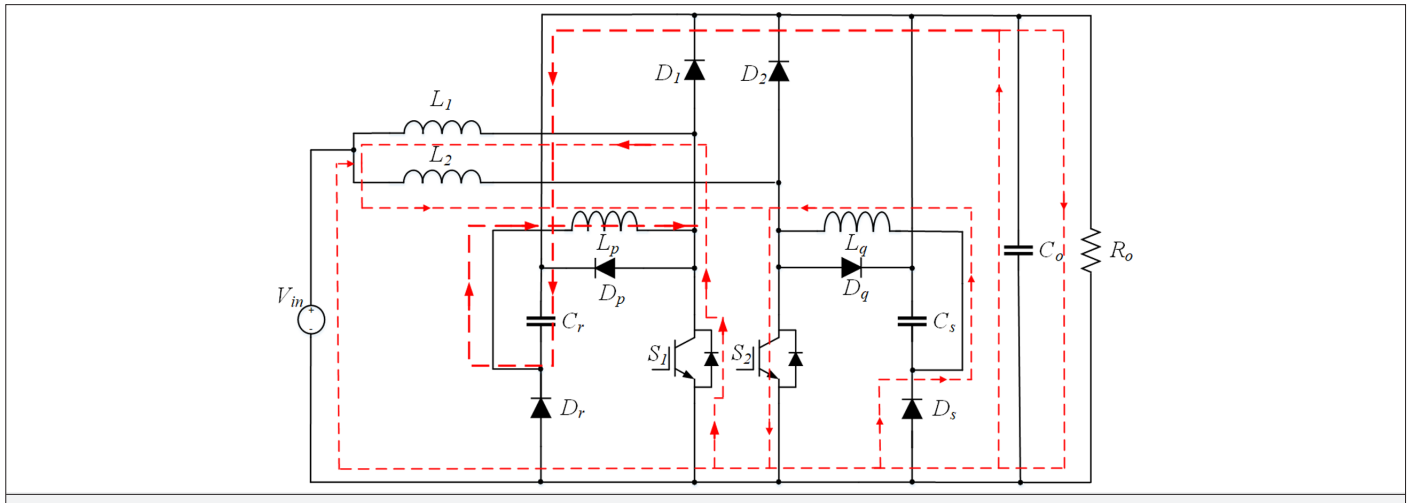

Fig. 4. Equivalent circuit: Interval-1 (t_0-t_1).

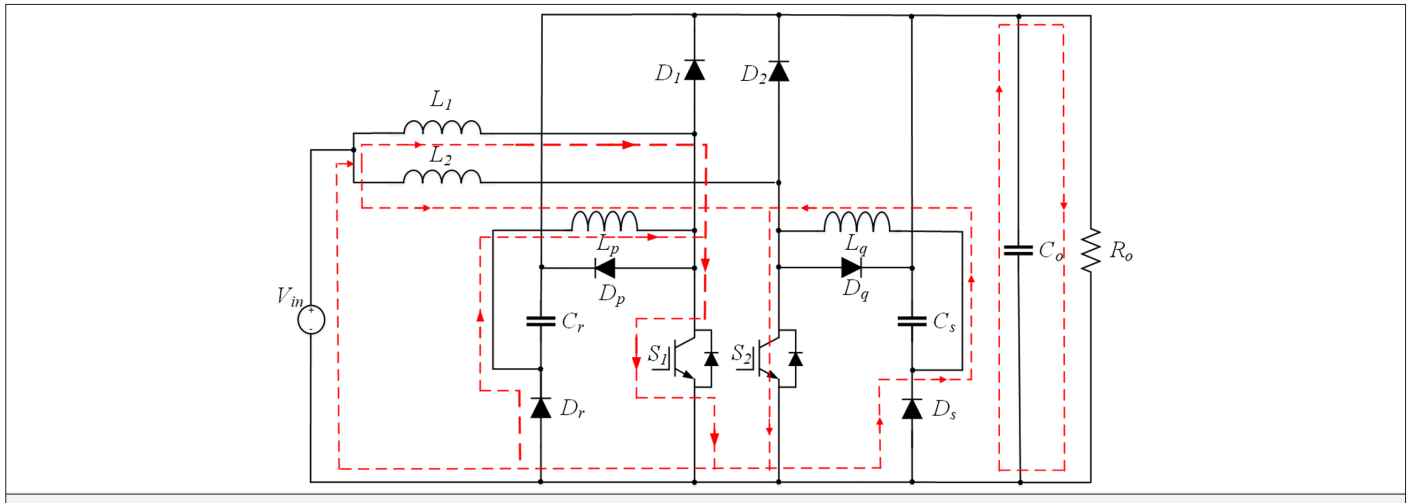

Fig. 5. Equivalent circuit: Interval-2 (t_1-t_2).

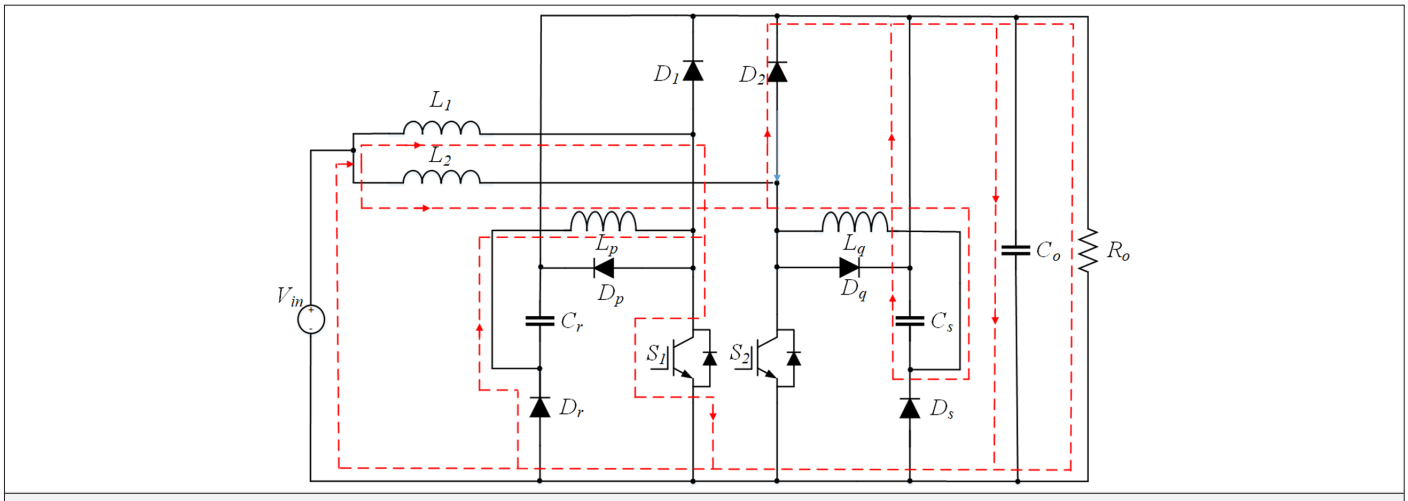

Fig. 6. Equivalent circuit: Interval-3 (t_2-t_3).

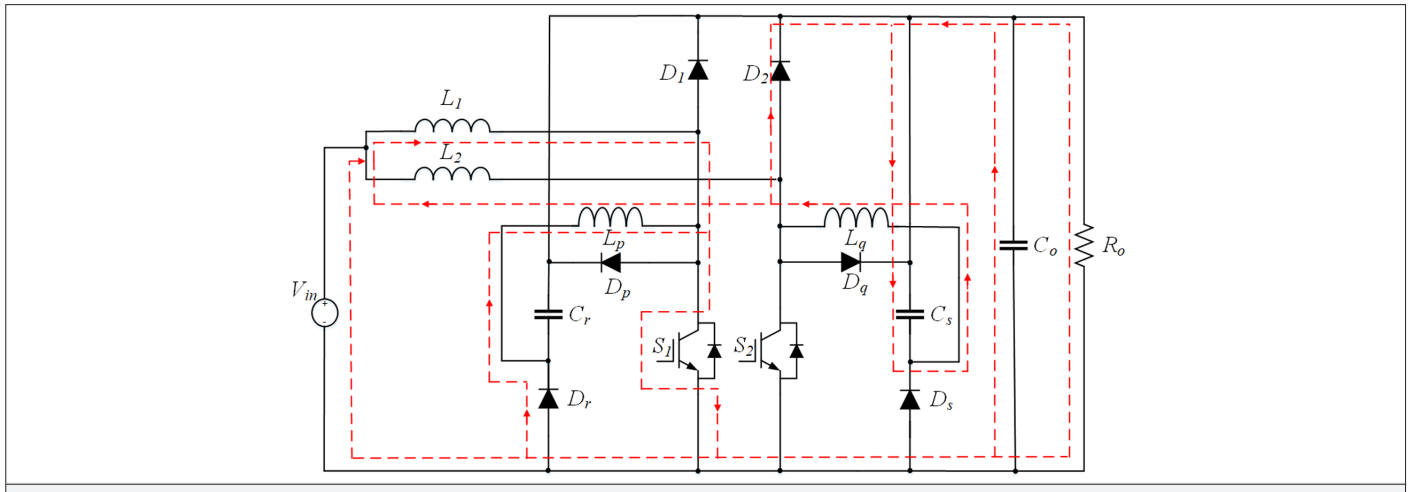

Fig. 7. Equivalent circuit: Interval-4 (t_3-t_4).

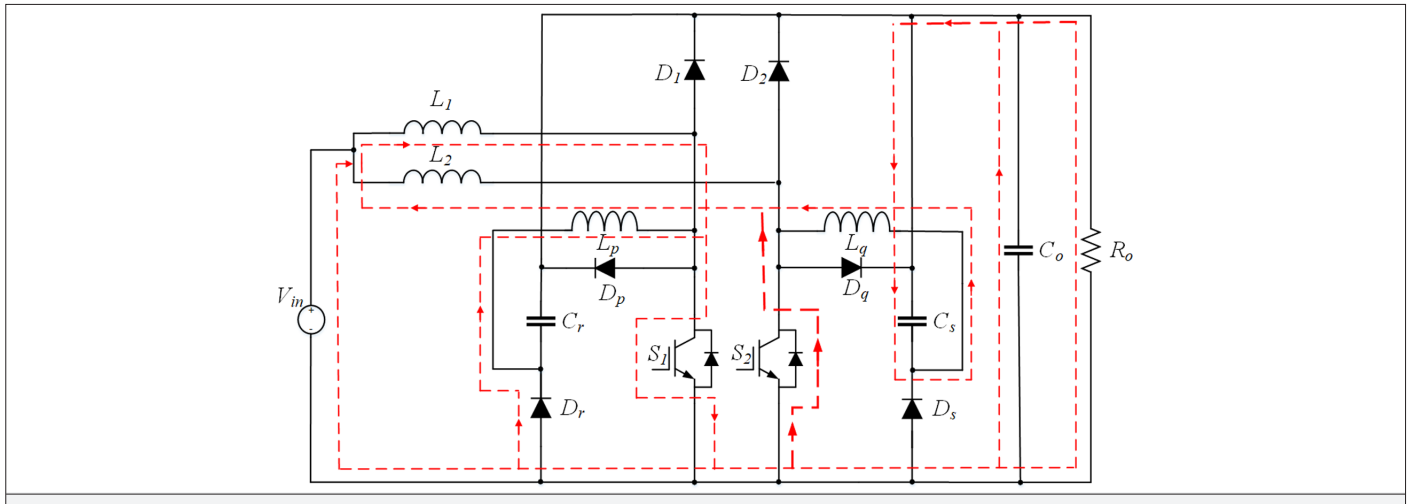

Fig. 8. Equivalent circuit: Interval-5 (t_4-t_5).

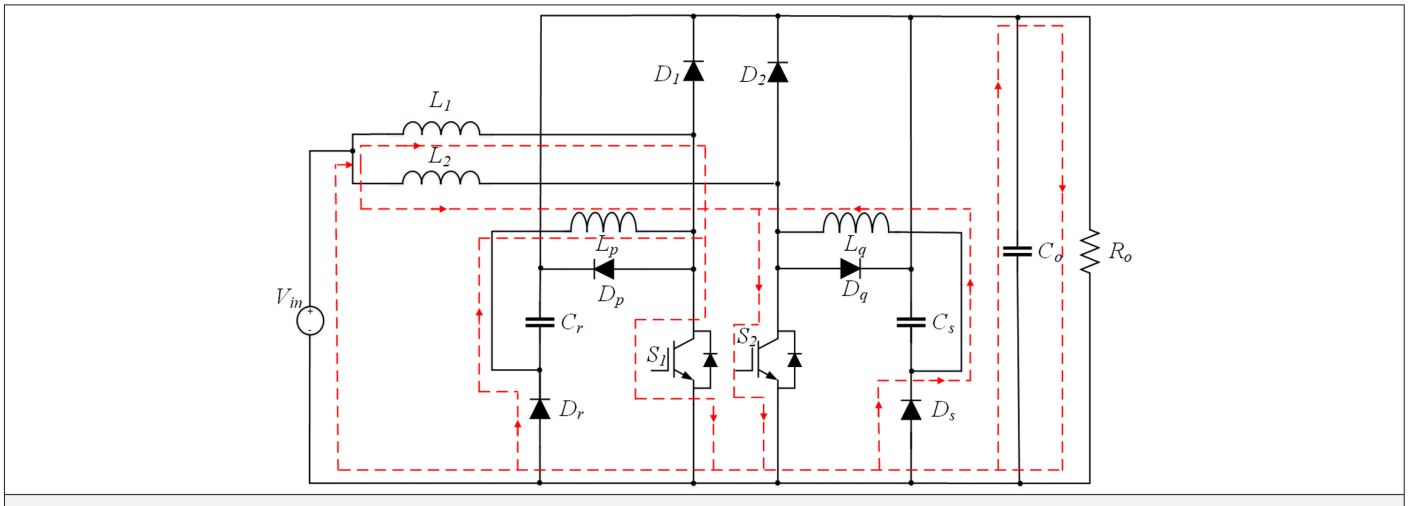

Fig. 9. Equivalent circuit: Interval-6 (t_5-t_6).

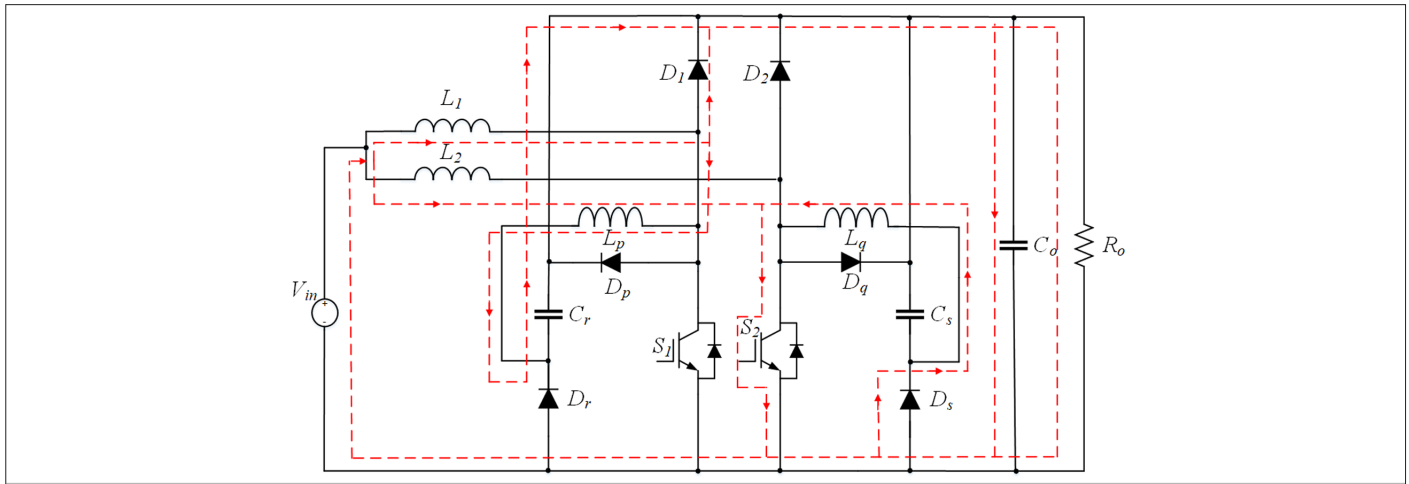

Fig. 10. Equivalent circuit: Interval-7 (t_6-t_7).

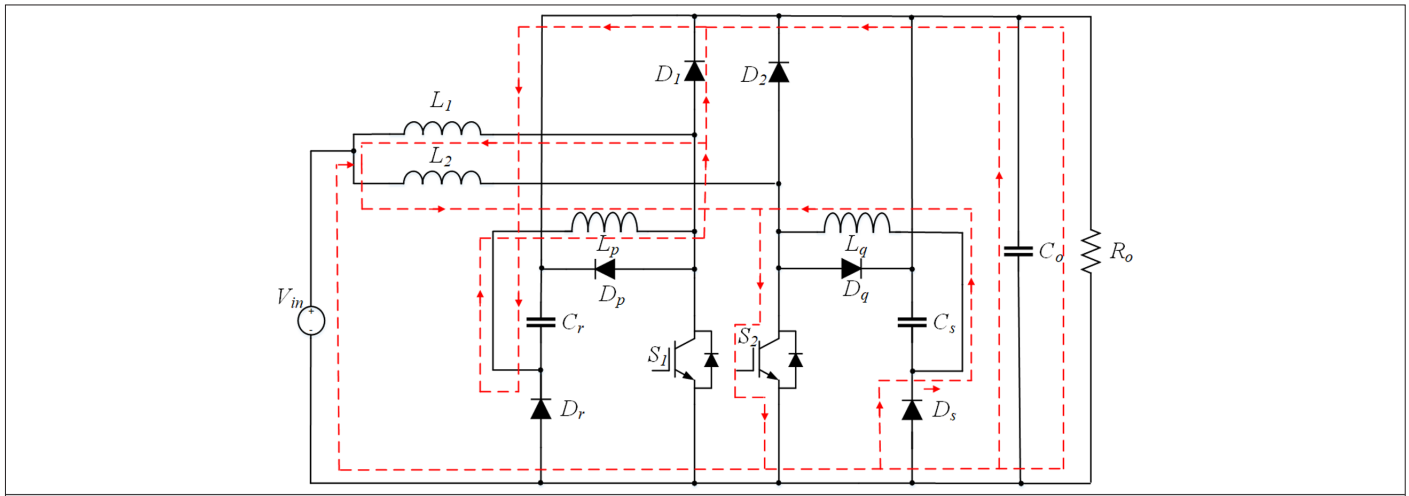

Fig. 11. Equivalent circuit: Interval-8 (t_7-t_8) and Interval-9 (t_8-t_9).

direction. Hence, the ZVS condition is achieved. S_2 was already in a conducting state prior to this interval. Throughout this interval, C_r is charging, and the current through L_p increases smoothly. At the end, the body diode of S_1 stops conducting.

Interval-2 (t_1-t_2): At t_1, S_2 is in the off state and S_1 is turned on. During this interval, C_r is charged to V_o, current through S_1 is at zero, i_{Lp} reaches $-I_o$, i_{Lq} changes from $-I_{o\ to\ +}I_o$, and C_s is in a discharging state. The governing equations for currents through the inductors, i_{Lp} and i_{Lq}, *current through the switch,iS1,* and voltages across the capacitors V_{Cr} and V_{Cs} are expressed as (1-5):

$$i_{Lp}(t) = -V_0\sqrt{\frac{C_r}{L_p}} \tag{1}$$

$$i_{Lq}(t) = -V_0\sqrt{\frac{C_s}{L_q}} \tag{2}$$

$$i_{S1}(t) = i_{L1}(t) \tag{3}$$

$$V_{cr}(t) = V_0 \tag{4}$$

$$V_{cs}(t) = V_0 \tag{5}$$

Interva1-3 (t_2-t_3): At t_2, S_1 is turned on under ZCS conditions, and energy begins to accumulate in L_1. The voltage across S_2 equals V_o, while i_{Lq} decreases linearly, and C_s is fully discharged. The equations for current through the switch i_{S1}, currents through the inductors, i_{Lp} and i_{Lq}, and voltages across the capacitors V_{Cr} and V_{Cs} are given by (6-10):

$$i_{S1}(t) = \frac{1}{L_1}V_{in}(t-t_2) + i_{L1}(t_2) \tag{6}$$

$$i_{Lq}(t) = (V_{in} - V_0)\sqrt{\frac{C_s}{L_2 + L_q}}\,\mathrm{Sin}\,\omega_0(t-t_2) + i_{L1}(t_2) \tag{7}$$

$$\omega_0 = \frac{1}{\sqrt{(L_q + L_2)C_s}}\; i_{Lp}(t) = -V_0\sqrt{\frac{C_r}{L_p}} \tag{8}$$

$$V_{Cs}(t) = V_0 - \left[\left(V_{in} - V_0 \right) \sqrt{\frac{C_s}{L_2 + L_q}} \right] \text{Sin}\,\omega_0 (t_2 - t_1) \tag{9}$$

$$V_{Cr}(t) = V_0 \tag{10}$$

Interval-4 (t_3-t_4): At t_3, due to resonance between L_q and C_s, S_2 voltage starts decaying smoothly. S_2 voltage smoothly falls to zero at the instant L_q reaches its maximum and C_q is completely charged. The equations for currents through the switches i_{S1} and i_{S2}, currents through the inductors, i_{Lp} and i_{Lq}, and voltages across the capacitors V_{Cr} and V_{Cs} are given by (11-16):

$$i_{S1}(t) = \frac{1}{L_1} V_{in}(t - t_3) + i_{S1}(t_3) \tag{11}$$

$$i_{S2}(t) = 0 \tag{12}$$

$$i_{Lq}(t) = (V_0 - V_{in}) \sqrt{\frac{C_s}{L_2 + L_q}}\, \text{Sin}\,\omega_0 (t - t_3) + i_{Lq}(t_3) \tag{13}$$

$$i_{Lp}(t) = -V_0 \sqrt{\frac{C_r}{L_p}} \tag{14}$$

$$V_{Cs}(t) = V_0 (1 - \cos \omega_0 (t - t_3)) \tag{15}$$

$$V_{Cr}(t) = V_0 \tag{16}$$

Interval-5 (t_5-t_6): At t_5, S_2 is turned on, and S_1 is still being conducted. Currents through L_p, L_q are at I_o, and C_r, C_s are at V_o.

Interval-6 (t_6-t_7): At t_6, S_1 is turned off and S_2 is conducting. Output power flows via the V_{in}-L_1-body diode of S_1. During this interval, C_s is charged to V_o, i_{Lq} reaches to $-I_o$, i_{Lp} changes from $-I_o$ to $+I_o$, and C_r is in a discharging state. The equations for currents through the switches i_{S1} and i_{S2}, currents through the inductors, i_{Lp} and i_{Lq}, and voltages across the capacitors V_{Cr} and V_{Cs} are given by (17-22):

$$i_{S2}(t) = \frac{1}{L_2} V_{in}(t - t_5) + i_{S2}(t_5) \tag{17}$$

$$i_{S1}(t) = 0 \tag{18}$$

$$i_{Lp}(t) = (V_0 - V_{in}) \sqrt{\frac{C_r}{L_1 + L_p}}\, \text{Sin}\,\omega_0 (t - t_5) + i_{Lp}(t_5) \tag{19}$$

$$i_{Lq}(t) = -V_0 \sqrt{\frac{C_s}{L_q}} \tag{20}$$

$$V_{Cr}(t) = V_0 (1 - \cos \omega_0 (t - t_5)) \tag{21}$$

$$V_{Cs}(t) = V_0 \tag{22}$$

Interval-7 (t_7-t_8): At t_7, S_2 is still turned on, and energy is accumulating in L_2. Voltage across S_1 equals V_o. i_{Lp} is linearly decreasing and C_r is completely discharged.

Interval-8 (t_8-t_9): At t_3, due to resonance between L_p and C_r, and S_1 voltage starts decaying smoothly. S_1 voltage smoothly falls to zero at the instant L_p reaches its maximum and C_r is completely charged.

III. DESIGN ANALYSIS

The converter operation is classified into two states to analyze the input current ripples of the converter. When S_1 is turned on, it is the first state and the second state is when both S_1 and S_2 are turned on.

State 1: During this state, when only S_1 is turned on, energy accumulates in the input inductor L_1. The input current is then delivered to the output through L_2, as S_2 remains off. The input current i_{in} is given by (23):

$$\frac{di_{in}}{dt} = \frac{V_{in}}{L} + \frac{V_{in} - V_o}{L} \tag{23}$$

State 2: In this state, both switching devices S_1, S_2 are turned on, allowing energy to accumulate in both inductors L_1, L_2. The input current, i_{in} is expressed as follows (24):

$$\frac{di_{in}}{dt} = \frac{V_{in}}{L} + \frac{V_{in}}{L} \tag{24}$$

Current through the inductor L_q is given by (25):

$$i_{Lb}(t) = i_o \cos\left(\frac{\pi}{2} + \omega (t - t_4) \right) \tag{25}$$

The average output voltage V_o is given by the following expression (26):

$$V_o = \frac{V_{in}}{1 - D} \tag{26}$$

The input voltage, V_{in} is expressed as (27):

$$V_{in} = V_o (1 - D) \tag{27}$$

By substituting (26) into (23), the input current, i_{in}, is expressed as (28):

$$\frac{di_{in}}{dt} = \frac{V_o}{L} \left(1 - 2D \right) \tag{28}$$

By substituting (26) into (24), the input current, i_{in}, is expressed as (29):

$$\frac{di_{in}}{dt} = \frac{V_o}{L} \left(2 - 2D \right) \tag{29}$$

The two operating cases are as follows: Case 1, when S_1 is the only switch in the conduction state ($0 < D < 0.5$), and Case 2, when both S_1 and S_2 are in the conducting state ($0.5 < D < 1$). In both operating cases, the input current ripple is given by (30):

$$\Delta i_{in} = \begin{cases} \frac{Vo}{L} (1 - 2D) D T_s ; 0 \le D \le \frac{1}{2} \\ \frac{Vo}{L} (2 - 2D) \left(D - \frac{1}{2} \right) T_s ; \frac{1}{2} \le D \le 1 \end{cases} \tag{30}$$

The input current ripple is given by (31):

$$\Delta i_{in} = \frac{Vo}{L} (2 - 2D) \left(D - \frac{1}{2} \right) T_s \tag{31}$$

The voltage gain of the converter is given by (32):

$$M = \left(\frac{V_o}{V_{in}} \right) \tag{32}$$

The output current (i_o) of the converter are given by (33):

$$i_o = \frac{M}{Q} \tag{33}$$

where $Q = \frac{R_o}{Z_o}$; characteristic impedance $Z_o = \sqrt{\frac{L_a}{C_a}}$

The input current (i_{in}) of the converter are given by (34):

$$i_{in} = i_o M = \frac{M^2}{Q} \tag{34}$$

The following condition must be satisfied to select the output resistance, R_o (35):

$$R_o \geq \frac{V_{in}}{(1-D)i_o} \tag{35}$$

For a Q factor of 3, the values of the resonant elements L_a, C_a, L_b, and C_b are chosen, and the characteristic impedance, Z_o, is set to 35 ohms.

The following condition must be satisfied to select the L_1 and L_2 (36):

$$L \leq \frac{V_{in}D}{\Delta i_{pv} f_s} \tag{36}$$

The output filter capacitance, C_o, is determined using the following equation (37):

$$C_o = \frac{DV_o}{R_o \Delta V_o f_s} \tag{37}$$

The maximum voltage stress of the IGBT is determined by (38):

$$V_{Stress\_IGBT} = V_{in}\left(\frac{M^2}{Q}\right) \tag{38}$$

The maximum current stress on the input inductors is determined by (39):

$$i_{L\max} = \frac{V_{in}\left(\frac{M^2}{Q}\right)}{Z_o} \tag{39}$$

IV. LOSS ANLAYSIS OF THE PROPOSED CONVERTER

This section presents the loss analysis of the proposed converter operating at 200 W output power, with a 48 V (V_{in}), 260 V(V_o), and an output current of 0.8 A.

A. Switch Losses

The peak current of the switch $i_{sw(peak)}$ is expressed as (40):

$$i_{sw(peak)} = \frac{1}{L_1} V_{in} \times DT_s \tag{40}$$

The rms current of the switch $i_{sw(rms)}$ is expressed as (41):

$$i_{sw(rms)} = i_{sw(peak)}\sqrt{\frac{D}{3}} \tag{41}$$

Power losses in switches during turn-off (42)

$$P_{sw} = i_{sw(rms)}{}^2 \times r_{(on)} + \frac{V_{sw} \times i_{sw(peak)} \times f_{sw} \times t_f}{6} \tag{42}$$

where $r_{(on)=}$ on state resistance

B. Inductor Losses

The rms current through L_1 ($i_{L1(rms)}$) is determined by (43):

$$i_{L1(rms)} = I_{in}\sqrt{D\left(1+\frac{\Delta i_L}{i_{L\min}}\left(1+\frac{1}{3}\times\frac{\Delta i_L}{i_{L\min}}\right)\right)} \tag{43}$$

where Δi_L= input ripple ; i_{Lmin}=minimum input current; I_o=output current

Power loss of the inductors is calculated by the following expression (44):

$$P_{Lloss(rms)} = I_{L(rms)}{}^2 \times r_L \tag{44}$$

where $r_{L=}$ inductor internal resistance

The rms current inductor ($i_{Lp(rms)}$) is calculated by (45):

$$i_{Lp(rms)} = \sqrt{\left(\frac{V_{Cr}}{2\pi^2}\times\frac{C_r}{L_p}\times D\right) + I_{in}^2(1-D-x)} \tag{45}$$

where $x = \frac{(V_{Cr}-V_{in})D}{2\pi I_o}\sqrt{\frac{C_r}{L_p}}(1-\cos 2\pi D)\times\left(\frac{1-D}{3}\right)$

Magnetic core losses for the inductors L_1, L_2 (46)

$$P_{Lloss(rms)} = K \times f_s^{\alpha} \times \Delta B^{\beta} \times V \tag{46}$$

where K=Steinmetz constant=5 × $10^{0-1-2-3}$; f_s= switching frequency=40 kHz; ΔB= Change in peak magnetic flux density=0.05 T; V=Volume of the core=10 cm^3

C. Diode Losses

The diodes D_1, D_2 rms currents ($I_{D1(rms)}$) are expressed as follows (47):

$$I_{D1(rms)} = \frac{2\sqrt{D}}{(1-D)}\times I_o\sqrt{1+\frac{1}{3}\left(\frac{\Delta I_L}{I_o}\right)^2} \tag{47}$$

The diodes D_1, D_2 average currents ($I_{D1(avg)}$) are expressed as follows (48):

$$I_{D1(avg)} = \frac{I_{peak}+I_{\min}}{2}\times(1-D) \tag{48}$$

The overall power loss ($P_{loss(rms)}$) of the diodes are as follows (49):

$$P_{loss(rms)} = I_{d(rms)}{}^2 \times r_d + V_\gamma \times i_{d(avg)} \tag{49}$$

where V_γ= forward voltage drop r_d= diode resistance

The diodes D_p, D_q rms currents ($I_{Dp(rms)}$) are given by (50):

$$I_{Dp(rms)} = \sqrt{\frac{1}{T_s}\int_0^{DT_s}\left(V_{Cr}\sqrt{\frac{C_r}{L_p}}\sin\left(\frac{2\pi}{T_s}t\right)\right)^2 dt} \tag{50}$$

The diodes D_p, D_q average currents ($I_{Dq(avg)}$) are given by (51):

$$I_{Dp(avg)} = \frac{V_{Cr}}{\pi}\sqrt{\frac{C_r}{L_p}} \times \frac{D}{3} \tag{51}$$

The total power losses of the diodes are calculated by (52):

$$P_{Dloss} = I_{d(rms)}{}^2 \times r_d + V_\gamma \times I_{d(avg)} \tag{52}$$

The diode D_r rms current ($I_{Dr(rms)}$) is given by (53):

$$I_{Dr(rms)} = I_{in} \times 0.4\sqrt{D} \tag{53}$$

The diode D_r average current ($I_{Ds(avg)}$) are given by (54)

$$I_{Dr(avg)} = I_{in} \times 0.4\left(\frac{D}{3}\right) \tag{54}$$

As seen in Table 1, (41)–(54) are used to calculate all losses, the total losses in the diodes are 3.76 W, in the inductors are 1.76 W, and in the capacitors are 0.09 W. The total switching power losses are 2.32 W.

V. SIMULATION RESULTS

The proposed soft-switched interleaved boost converter is designed and simulated using the PLECS simulation tool. The values of parameters used for simulation are as follows: input voltage (V_{in}): 48 V, switching frequency (f_{sw}): 40 kHz, output voltage (V_o): 260 V, inductors L_1, L_2 = 100 µH, resonant inductors L_p, L_q = 1.5 µH, resonant capacitors, C_p, C_q = 20 nF and output capacitor C_o = 470 µF. The voltage and current waveforms of IGBTs S_1, S_2 are shown in Fig. 12(a, b, c, d). As per obtained waveforms, the voltages across IGBTs smoothly reach zero and hence the ZVS condition is obtained without introducing any further voltage or current stresses. Fig. 13 shows i_{Lp}, i_{Lq}, and V_{Cr}, V_{Cs}. The obtained waveforms of resonant capacitors C_p, C_q confirm that the voltage across capacitors is equal to the output voltage V_o. Average current through the resonant inductors L_p, L_q is equal to the output current.

VI. EXPERIMENTAL RESULTS

The proposed converter 48 V/260 V is developed and verified experimentally at 200 W output power. The parameters used to develop the laboratory prototype are illustrated in Table 2. The Pulse Width Modulation (PWM) signals are generated using Texas Instruments TMS320F28335. The Infineon IGBTs IHW25N120R2 with 1200 V/25 A are used as S_1, S_2. Ferrite core of E-70 type is used to design 100 µH inductors, L_1, L_2 and L_p, L_q. Polypropylene (PP) film capacitors, FKP2O111001I00, are used as resonant capacitors C_r and C_s. WOLFSPEED SiC SCHOTTKY C6D06065A diodes, D_1, D_2, D_p, D_q, D_r, and D_s, are used in the prototype. All the experimental results were measured under steady-state operation, while the converter input current was continuous with an input voltage of 48 V.

Fig. 14 shows the obtained collector-emitter voltage and collector current waveforms of the main switches S_1, S_2. It can be seen from these results that ZVS turn-on is achieved, and the voltage across the main switching devices is equal to the output voltage, while the converter achieves a 260 V output voltage with a 48 V input voltage. Hence, the voltage stresses are lower, and the turn-on losses are also reduced. The voltage and current measured waveforms of S_1, S_2 are the same as the simulated results, except for their body diode conduction. Fig. 15 shows the current flows through the L_p and L_q. It is observed that when the main switches are turned off, the maximum peak current equals the output current, 0.65 A, and becomes zero during the turn-on condition of the main switches. The voltage across the resonant capacitors C_p, C_q shown in Fig. 16. The voltage across both capacitors, C_p, C_q, is continuously charging to a maximum of 260 V and discharging when the main switches are turned off. The main advantage of this is that the converter achieves soft-switching without the need for auxiliary switches and coupled inductors.

The proposed converter was verified on three different input voltages: 30 V, 40 V, and 48 V. Fig. 17 shows the clear turn-on and turn-off transitions of S_1, S_2 while the converter is operated with a 30 V input voltage and a 155 V obtained output voltage. Fig. 18 shows the clear turn-on and turn-off transitions of S_1, S_2 while the converter is operating with a 40 V input voltage and a 215 V obtained output voltage. Fig. 19 shows clear turn-on and turn-off transitions of S_1, S_2 while the converter is operating with a 48 V input voltage and a

TABLE 1. LOSS CALCULATION OF THE PROPOSED CONVERTER

Device Type	Components	$r_{(on)}$ (mΩ)	V_{max} (V)	V_γ (V)	I_{rms} (A)	I_{avg} (A)	Loss (W)
Diode	D_1, D_2	10	250	1.25	3.9	1.5	2.1
	D_p, D_q,	10	250	1.25	4.2	0.735	1.23
	D_r, D_s,	10	250	1.25	1.372	0.38	0.38
Switch	S_1, S_2	30	260	–	4.05	–	2.32
Inductor copper losses	L_1, L_2	20	–	–	4.5	–	0.81
	L_p, L_q,	20	–	–	4.92	–	0.96
Magnetic core losses	L_1,L_2	20	–	–	–	–	0.023
	L_p, L_q,	20	–	–	–	–	0.01
Capacitor	C_r, C_s, C_o	80	260	–	0.3	–	0.09
							7.93

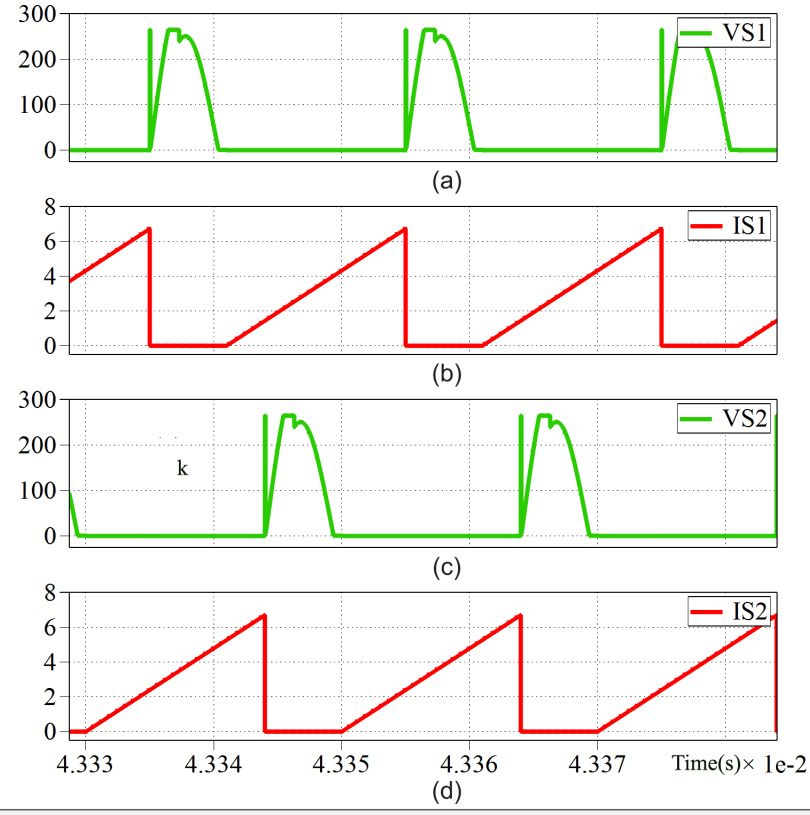

Fig. 12. PLECS simulation waveforms. (a) V_{S1}. (b) i_{S1}. (c) V_{S2}. (d) i_{S2}.

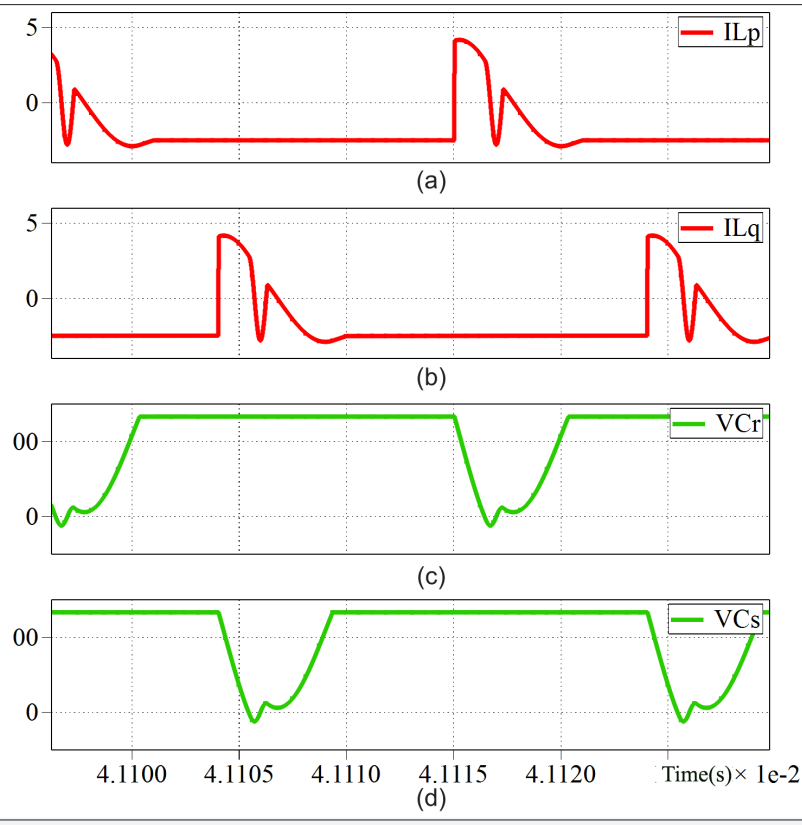

Fig. 13. PLECS simulation waveform results. (a) i_{Lp}. (b)i_{Lq}. (c)V_{Cr}. (d) V_{Cs}.

TABLE 2. PROTOTYPE PARAMETERS

Parameter	Symbol	Value
Input voltage	V_{in}	48 V
Output voltage	V_o	260V
Output power	P_o	250 W
Switching frequency	f_{sw}	40 kHz
Resonant inductors	L_p, L_q	1.5 µH
Resonant capacitors	C_r, C_s	20 nF
Inductors	L_1, L_2	100 µH
Output capacitor	C_o	470 µF
IGBTs	S_1, S_2	IHW25N120
Diodes	$D_1, D_2, D_p, D_q, D_r, D_s$	C6D06065A

IGBTs, Insulated Gate Bipolar Transistors.

260 V output voltage. The difference can be seen in the collector-emitter voltage waveform of S_1, S_2 at 155 V as it smoothly falls to zero, whereas at 260 V, the collector-emitter voltage waveform linearly decreases to zero. The obtained efficiency of this converter is 96% at a 200 W output power level. Table 3 illustrates the comparison of the proposed converter with existing topologies [12] [15] [17] [25]. The advantages and disadvantages of the existing topologies and the proposed topology are summarized in Table 4. The major benefit of this proposed converter is that it is designed without auxiliary switches, thus avoiding control complexity to drive the switches. The converter has the following advantages over the existing converters: no auxiliary switches, simple control, reduced switching losses, reduced voltage stresses, and improved efficiency. Fig. 20 shows the overall distribution of the proposed converter. The total power loss of the proposed converter is 7.9 W when operating at an output power of 200 W, resulting in an overall efficiency of 96%. Fig. 20 presents a pie chart illustrating the loss distribution within the converter. Fig. 21 compares the efficiency of the proposed topology with existing topologies. Fig. 22 shows the measured efficiency curve of the proposed interleaved converter, where a maximum efficiency

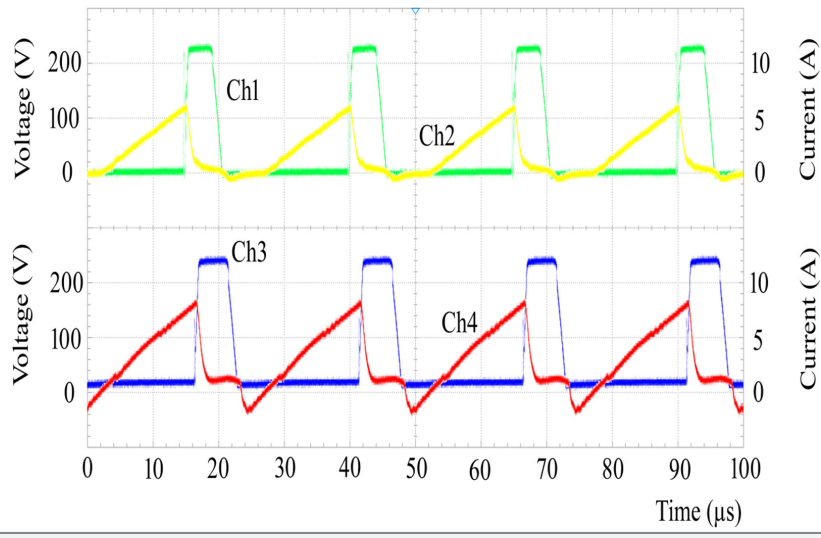

Fig. 14. Experimental waveforms. Ch1 (100 V/div): S_1 collector-emitter voltage. Ch2 (5 A/div): S_1 collector current (Top). Ch3 (100 V/div): S_2 collector-emitter voltage. Ch4 (5 A/div): S_2 collector current (Bottom).

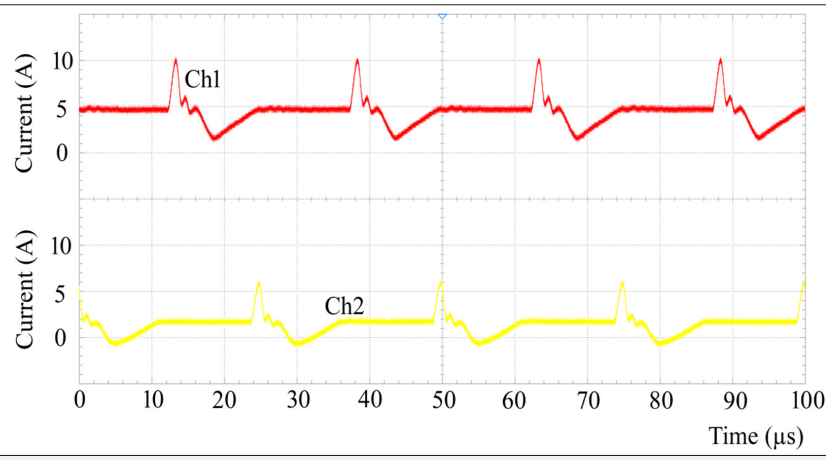

Fig. 15. Experimental results. i_{Lp}: Current through resonant inductor L_p Ch1: 5A/div (Top) i_{Lq}: Current through resonant inductor L_q Ch2: 5A/div (Bottom) (Time scale: 10 µs/div).

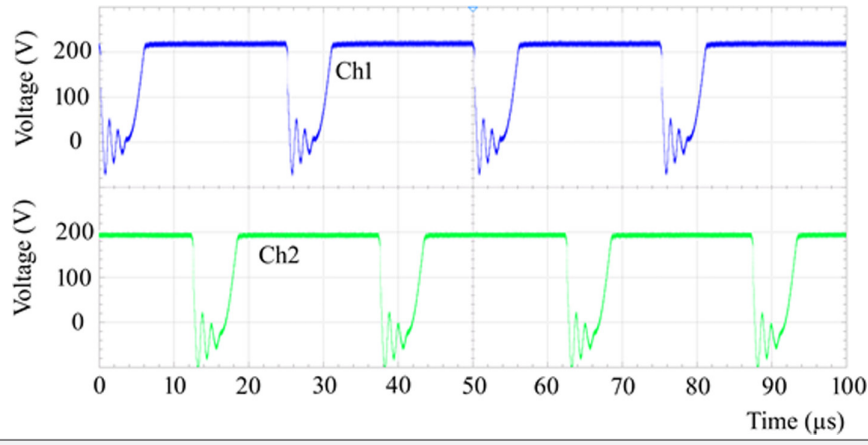

Fig. 16. Experimental results. V_{Cp}: Voltage across C_p Ch1: 100V/div (upper) V_{Cq}: Voltage across C_q Ch2: 100V/div (bottom) (Time scale: 10 μs/div).

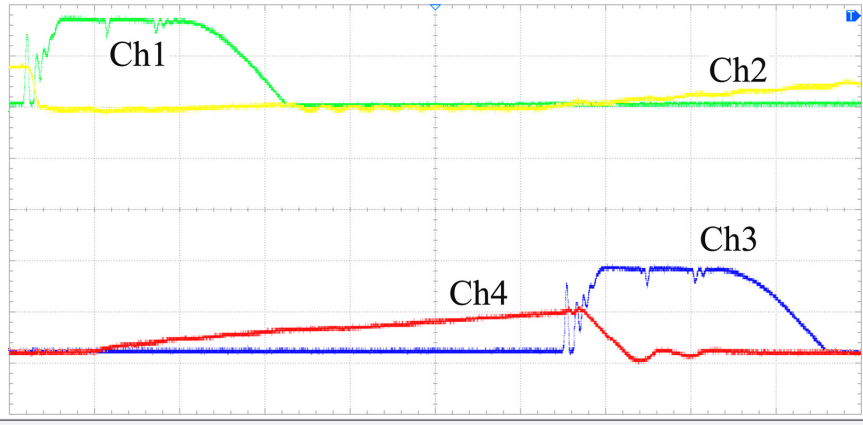

Fig. 17. Experimental results. $V_{in} = 30$ V; $V_o = 150$ V_{S1}: Collector-emitter voltage Ch1: 100V/div i_{S1}: Collector current Ch2: 5A/div (Top). V_{S2} : Collector-emitter voltage Ch3 Ch3: 100V/div i_{S1}: Collector current Ch4: 5A/div (Bottom) (Time scale: 2 μs/div).

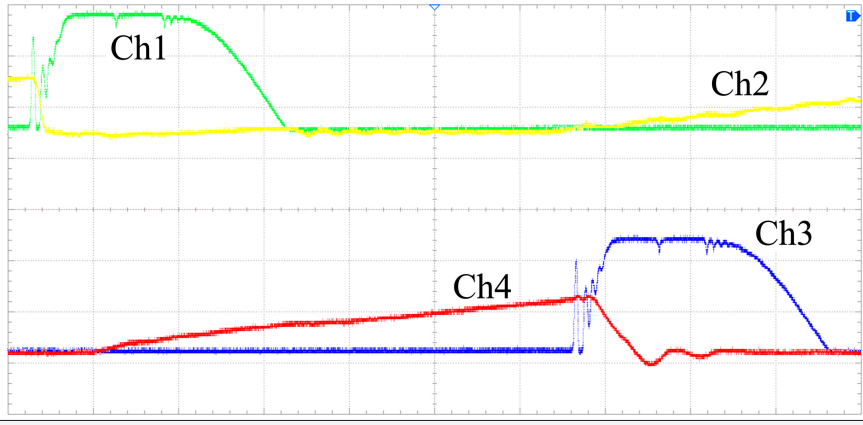

Fig. 18. Experimental results. $V_{in} = 40$V $V_o = 215$V V_{S1}: Collector-emitter voltage Ch1: 100V/div i_{S1}: Collector current Ch2: 5A/div (Top). V_{S2} : Collector-emitter voltage Ch3 Ch3: 100V/div i_{S1}: Collector current Ch4: 5A/div (Bottom) (Time scale: 2 μs/div).

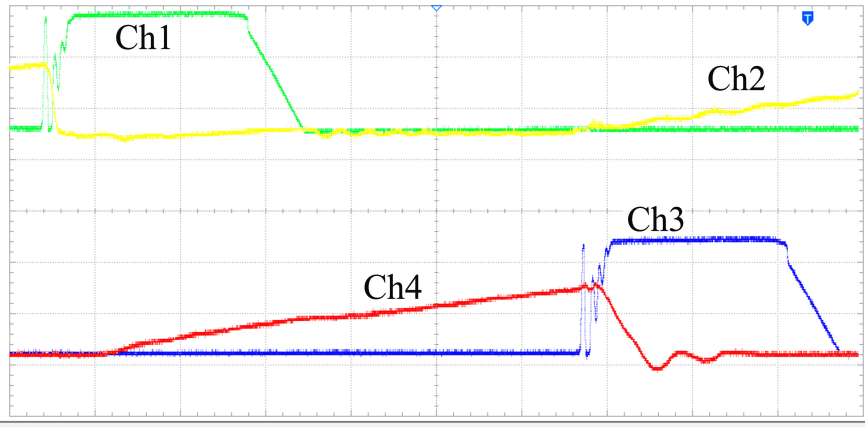

Fig. 19. Experimental results. V_{in} = 48 V V_{out} = 260 V V_{S1}: Collector-emitter voltage Ch1: 100 V/div i_{S1}: Collector current Ch2: 5 A/div (Top). V_{S2} : Collector-emitter voltage Ch3: 100 V/div i_{S1}: Collector current Ch4: 5 A/div (Bottom) (Time scale: 2 μs/div).

TABLE 3. COMPARISON OF EXISTING CONVERTERS WITH PROPOSED CONVERTER

	NS	NL	NC	ND	f_s (kHz)	V_{in}	V_o	P_o(W)	SS	TD	Efficiency (%)
[12]	5	5	8	8	100	46	850	2500	Yes	26	98.3
[15]	4	1, 1*	3	2	60	200	400	1200	Yes	11	95
[17]	3	3*	4	3	100	48	400	400	Yes	13	98
[25]	2	4	5	6	30	200	400	1200	Yes	17	97.2
Proposed	2	4	3	6	40	48	260	200	Yes	15	96

fs, switching frequency; NC, number of capacitors; ND, number of diodes; NL, number of inductors; NS, number of switches; P_o, output power; SS, soft-switching; TD, total device count; V_{in}, input voltage; V_o, output voltage.
*Coupled inductors.

TABLE 4. ADVANTAGES AND DISADVANTAGES: EXISTING CONVERTERS VERSUS PROPOSED TOPOLOGY

	Advantages	**Disadvantages**
[12]	• Reduced switching losses due to ZVS • High gain • Reduce input current ripple • Suitable for high power applications	• Increased control complexity • Higher device count • Increased cost and volume • Not suitable for low-power applications
[15]	• Reduced switching losses due to ZVS • Reduced switching stresses • Simple structure • Lower cost and size	• Electro-magnetic interference (EMI) • Increased turn-off losses • Soft-switching achievable only at lower switching frequencies • Not suitable for high-power applications
[17]	• Reduce switching losses • High gain • Reduced current ripple • High power density	• Control complexity • Increased size and weight • Increased component count • Not suitable for low-power applications
[25]	• Reduce switching losses • Reduced input current ripple • Reduced output voltage ripple • Improved efficiency	• Specific to certain applications • Implementation complexity • Expensive • Not suitable for high-power applications
Proposed topology	• Reduce switching losses due to ZVS • Less number of device count • Simplified control • Improved efficiency	• Increased turn-off losses • Increased size and weight • Suitable for both low and high power applications

ZVS, zero-voltage switching.

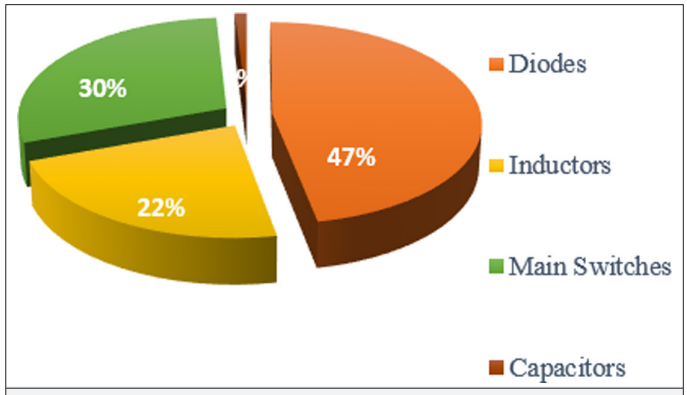

Fig. 20. Loss distribution of the proposed converter.

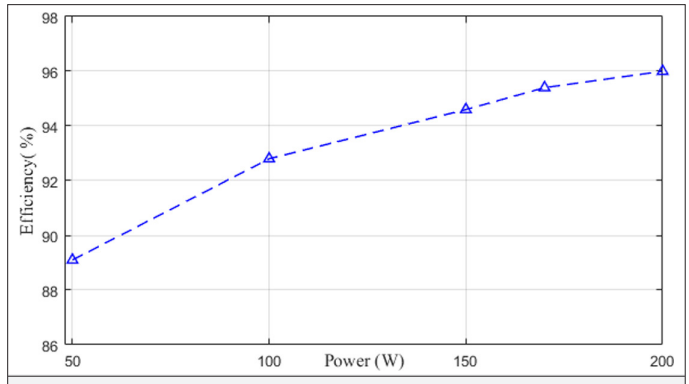

Fig. 22. Efficiency curve of the proposed topology.

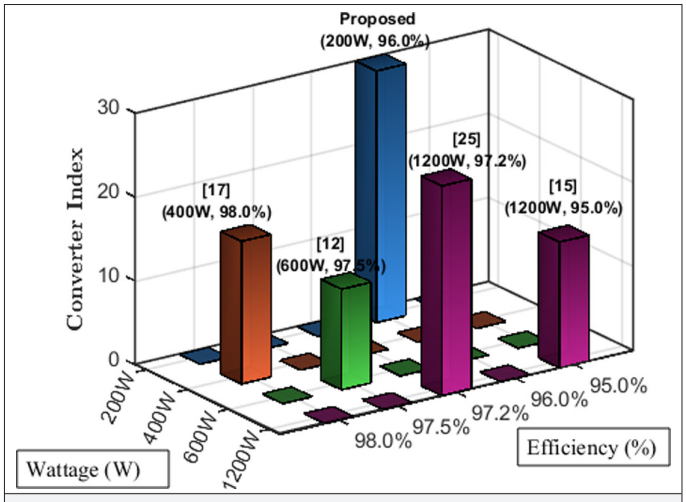

Fig. 21. Efficiency comparison between the proposed topology and existing topologies.

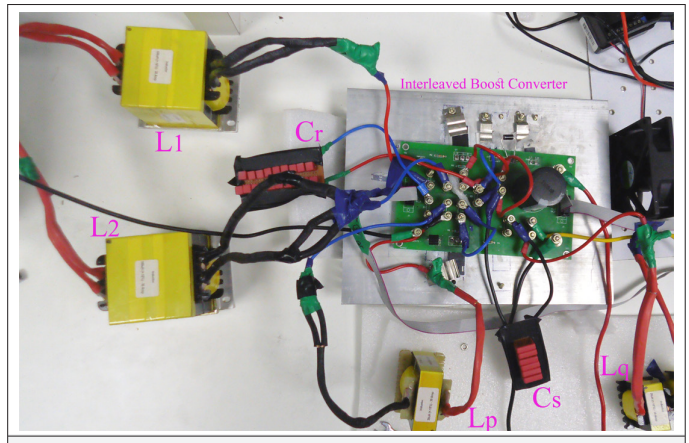

Fig. 23. Laboratory prototype used for experimental verification.

of 96% is achieved at an output power of 200 W. Fig. 23 shows the laboratory prototype used for the experimental verification of the proposed converter.

VII. CONCLUSION

This paper introduces a novel two-phase interleaved boost converter equipped with a simple auxiliary cell. The design analysis and operating principles of the converter are thoroughly described. Zero-voltage switching is successfully achieved without introducing additional losses. Experimental investigations were carried out on a 200 W laboratory prototype, which operates with an input voltage of 48 V and produces an output voltage of 260 V. The soft-switching capability of this converter was tested under three different input voltages: 30 V, 40 V, and 48 V. The simple auxiliary cell plays a critical role in ensuring ZVS turn-on of the IGBTs, contributing significantly to achieving a high efficiency of 96%. Compared to existing converters, the proposed design reduces the number of components, including auxiliary switches, thereby lowering the overall cost. This makes the proposed converter particularly suitable for high-power applications, such as photovoltaic conversion systems. Future work may focus on reducing the number of passive components and auxiliary switches, which could further enhance overall efficiency.

Data Availability Statement: The data that support the findings of this study are available on request from the corresponding author.

Peer-review: Externally peer-reviewed.

Author Contributions: Concept – V.V.S.K.B.; Design – V.V.S.K.B.; Supervision – P.D., V.K.; Resources – V.V.S.K.B.; Materials – V.V.S.K.B.; Data Collection and/or Processing – V.V.S.K.B., P.B; Analysis and/or Interpretation – V.V.S.K.B., P.B.; Literature Search – V.V.S.K.B.; Writing – V.V.S.K.B.; Critical Review – P.D., P.B, V.K.

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Veera Venkata Subrahmanya Kumar Bhajana received his degrees B.E. in Electronics and Communication Engineering from Sapthagiri College of Engineering, India (University of Madras), in 2000, M.E. from the P.S.N.A. College of Engineering and Technology under Anna University in the year 2005, and PhD in Electrical Engineering from Bharath University, India, in 2011. He was previously associated as a post-doc researcher at the University of West Bohemia, Pilsen, Czech Republic, from August 2013 to June 2015. He is currently working as an Associate Professor in the School of Electronics Engineering at KIIT (Kalinga Institute of Industrial Technology) University, Bhubaneswar, India, since December 2011.

Pravat Biswal was born in Bhubaneswar, India. He received the B.Tech. degree in electrical engineering from C.V. Raman College of Engineering at Bhubaneswar, Odisha, India, in 2008, and the M.Tech. degree from NIT Warangal specialized in power electronics and drive in 2011. He is currently a Ph.D. Research Scholar and an Assistant Professor with KIIT University, Odisha

Pavel Drabek received his M.S. and PhD degrees in electrical in electrical engineering from the University of West Bohemia (UWB), Pilsen, Czech Republic, in 2000 and 2004, respectively. From 2003 to 2005, he was a Design Engineer with the company Alltronic, Ltd., Pilsen. In 2005, he joined the UWB as an Assistant Professor in the Department of Electromechanics and Power Electronics, Faculty of Electrical Engineering. His main research interests include soft-switching inverters, ac-ac converters, multilevel converters, and electromagnetic compatibility of power electronic converters.

VIJAY KAKANI received the B.Sc. degree in electronics and communication engineering from Jawaharlal Nehru Technological University, Kakinada, India, in 2012, the M.Sc. degree in computers and communication systems from the University of Limerick, Ireland, in 2014, and the Ph.D. degree in information and communication engineering and future vehicle engineering from Inha University, South Korea, in 2020. He is currently an Assistant Professor in the Department of Integrated System Engineering, School of Global Convergence Studies, Inha University. His research interests include autonomous vehicles, sensor signal processing, applied computer vision, deep learning, systems engineering, and machine vision applications.