İSTANBUL UNIVERSITY CERRAHPAŞA

ORIGINAL ARTICLE
Electrica 2024; 24(1): 12-24

Design of a High-Efficiency Micro-Inverter with TO-220 Packaged Gallium Nitride - High-Electron-Mobility Transistors

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Cite this article as: T. Dayioglu, M.O. Gulbahce, A. Lordoglu and D. Ahmet Kocabas, "Design of a high-efficiency micro-inverter with TO-220 packaged gallium nitride - high-electron-mobility transistors," *Electrica*, 24(1), 12-24, 2024.

ABSTRACT

Since solar power panels generate direct current (DC) voltage, inverters are needed to provide DC/alternating current (AC) conversion to obtain suitable AC voltage forms for daily life and grid. Due to the disadvantages of central and string inverter systems, the use of micro-inverter systems is increasing nowadays. In micro-inverters, the use of new-generation gallium nitride-high-electron-mobility transistors (GaN-HEMTs), which has reached commercial maturity, has opened new horizons in solar power plant applications. GaN-HEMTs have low on-state resistance and high breakdown voltage and allow higher switching frequencies. This paper presents a detailed design methodology and analysis of a GaN-HEMT-based 250-W full-bridge micro-inverter. The LCL filter is designed to reduce the harmonic content of the output voltage and current of the inverter. Since more effort is required in layout design to take full advantage of ultra-fast switching GaN devices, layout design has been carefully completed for a better switching efficiency. The performance of the designed prototype was tested with and without the output filter for different power, voltage, and switching frequencies. The efficiencies for the rated operation at 50 kHz and 100 kHz switching frequencies were measured to be 97.5% and 96%, respectively.

***Index Terms*—**Gallium nitride-high-electron-mobility transistors, micro-inverter, solar system, wide band gap devices.

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Received: September 23, 2022

Revision Requested: January 29, 2023

Accepted: May 24, 2023

Publication Date: November 30, 2023

DOI: 10.5152/electrica.2023.22162

I. INTRODUCTION

The harmful effects of fossil fuel emissions and the phenomenon of global warming have brought renewable and clean energy resources to the fore. Photovoltaic systems (PV), which do not emit CO_2, have an important place in renewable energy sources, since they have a modular structure with no moving parts [1, 2]. PVs are still expanding rapidly, with incentives increasingly seen in our country and the world.

There are basically two different system types in PV power plants: standalone (off-grid) and grid connected (on-grid). Since solar energy is intermittent, an energy storage element (in other words, a battery) is added to the system in order to ensure the continuity of energy in off-grid systems, while there is no need to use batteries in grid-connected systems. Therefore, the generated extra electrical energy is directly transferred to the network on grid-connected systems that gained great importance in recent years due to their significantly reduced costs [3].

PV power systems include PV panels, inverters, and auxiliary electronic circuits. Previously known connection configurations of inverters are basically classified as centralized, string, and multi-string technologies (which are still being used), and in recent years, micro-inverter technology was introduced as can be seen in Fig. 1.

The centralized technology has one inverter connected to all PV panels accommodating its own maximum power point tracking (MPPT) algorithm, and it is used in high-power solar power plants. High-voltage direct current (DC) cabling is used for connecting the central inverter, and this brings about cable and diode losses as its disadvantages. The other types are string and multi-string technologies which are similar to each other. These technologies have no diode loss in series and offer distinct MPPT control for each string. The last type of up-to-date connection is

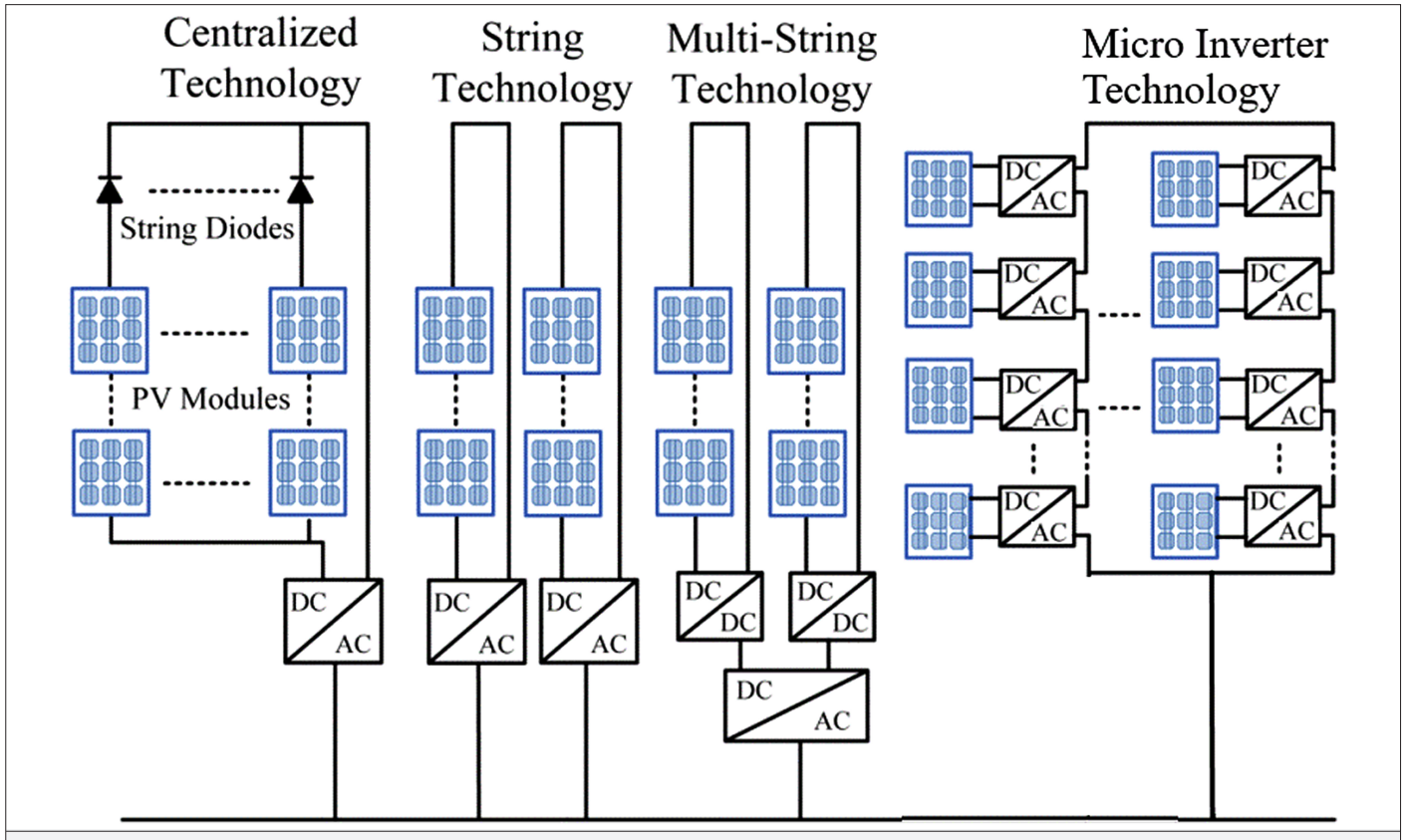

Fig. 1. PV power plant different connection configurations. PV, photovoltaic.

micro-inverter technology, which has still been widely used since the early 2010s. A number of relatively low-power (100–300 W) inverters, so-called micro-inverters, are connected to individual PV panels, and then all inverter outputs are connected to an AC bus. The word "micro" comes from its low power level and each micro-inverter has its own MPPT algorithm [3-5].

Previous technologies have many disadvantages. A single PV panel affected by ghosting, a faulty PV panel, or a diode fault will directly affect the overall system efficiency, reliability, and robustness [5]. The size and cost of circuit elements required for DC connection are relatively increased while system installation is relatively easier.

Micro-inverters have many advantages in terms of efficiency, cost of DC components, low heating, size, cost, and reliability [4, 5]. Every single PV module has its own inverter which reduces the installation costs. The micro-inverter systems are more cost-effective since there are no DC voltage cables and equipments while eliminating long installation processes and the need for well-trained workers [5]. The reliability of the system can be increased from 5 to 20 years by removing the coolants and reducing the operational temperature of the inverter [5]. Another important thing is the lifetime related to capacitor choice. Film capacitors provide a longer lifetime than electrolytic capacitors related to temperature durability [6] since the lifetime of an electrolytic capacitor is reduced to 20 000 hours when the temperature reaches 85°C [5].

In recent years, wide-band-gap semiconductors such as gallium nitride (GaN), high-electron-mobility transistors (HEMT) and silicon carbide (SiC) devices have been investigated comprehensively for power electronic systems [7-11]. The main advantage is their immensely fast switching speed, much further than that of the state-of-the art Si (silicon) semiconductor devices. Thus, in a power electronics circuit, the switching frequency can rise to very high levels in order to minimize the passive circuit elements and obtain less harmonic content, especially in micro-inverter applications, while keeping the efficiency high [12-14]. The important device properties of GaN are presented in Table I [7] in comparison with the conventional Si and SiC semiconductor devices. The saturation limit of GaN is far beyond Si and SiC as shown in Fig. 2 [15-18].

GaN has a superior relationship between on-resistance and breakdown voltage than that of Si devices due to higher electrical field strength and enhanced mobility of electrons in the two-dimensional electron gas. This means that GaN has the smallest drain-to-source on-resistance ($R_{ds(ON)}$) and the highest breakdown voltage for a certain power density. Besides, GaN semiconductor devices are very suitable for use in high-voltage applications, thanks to their high electrical

TABLE I. COMPARISON OF IMPORTANT DEVICE PROPERTIES OF GAN, SI, AND SIC SEMICONDUCTOR DEVICES

Properties	GaN	SiC	Si
Bandgap, EG (eV)	3.4	3.2	1.12
Breakdown field, EB (MV/cm)	3.3	3.5	0.3
Saturated drift velocity, Vs (10^7cm/s)	2.5	2.0	1.0
Electron mobility, μ (cm^2/Vs)	2000	650	1500

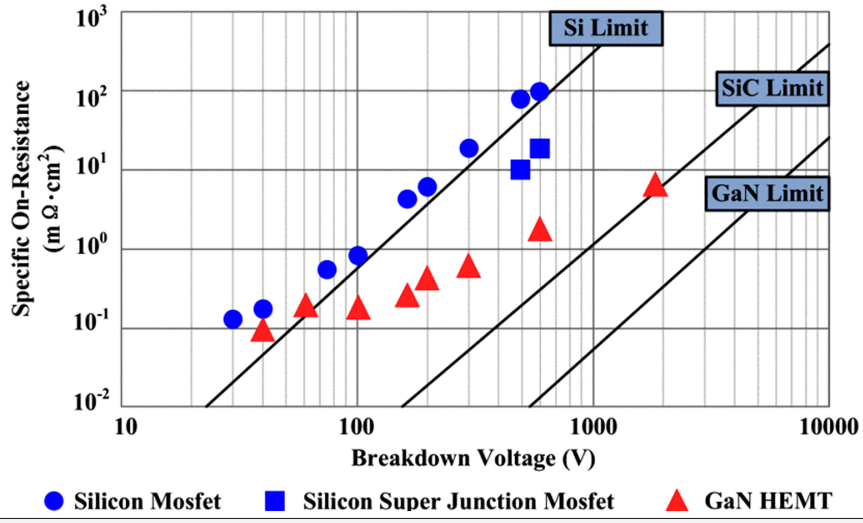

Fig. 2. On-resistance vs. breakdown voltage for semiconductor devices.

bandwidth and high breakdown voltage [13]. Relatedly, conduction losses are lower and efficiency is higher than that of the Si devices [12-14]. It has a low parasitic capacitance and low loss bringing about the thermal advantage that reduces heatsink dimensions. They also provide an advantage in terms of total weight and volume [19].

This study presents the design and practical implementation of a highly efficient micro-inverter design with new generation power devices providing 250 W rated power and 80 V (rms) output voltage. First, the analytical design of the micro-inverter was completed, and circuit components including power devices were chosen accordingly. Then, the design was simulated with an analytical power loss model of the selected GaN HEMT. In this stage, the results were interpreted to minimize the parasitic effects and the layout was completed. An LCL filter was designed for suppressing the dominant harmonics in output voltage and current. The bipolar sinusoidal pulse width modulation technique was also used to obtain low harmonic content at the output voltage. C2000 Piccolo TMS320F28027 DSP-based microcontroller was used for all software algorithms of the micro-inverter. In the practical stage, the circuit was tested under different operational conditions and analytical calculations and simulation results were seen to be in great harmony. No special attention was paid to DC–DC converters which are connected between micro-inverters and solar panels.

II. A SHORT OVERVIEW OF GAN HEMT DEVICES

A. Different GaN Types

Since, GaN HEMT has much lower junction capacitance and gate charge than that of Si MOSFET, faster turn-on/off is ensured and the junction capacitor stores less energy during the turn-off period. By means of these characteristics, the voltage and current transition interval is shortened and switching loss is decreased. Mainly, the high performance of GaN HEMTs ensures operating at higher switching frequencies than that of an Si MOSFET with the same efficiency. Furthermore, higher switching frequencies help to decrease the volume of the passive components and to increase the power density [16-18].

Many studies have shown that the normally-on (depletion) mode operation of GaN HEMT is not convenient for power-switching applications related to its requirements for fail-safe operation. On the other hand, the range of driving voltage for a normally-off GaN transistor is between (−5 V) and (+6 V) which is restricted by gate leakage current, making the GaN-based metal oxide semiconductor one of the candidates for normally-off (enhancement) devices. However, the safety of the driving limit is very low and the driving circuit must be designed crucially [16-18].

A low-voltage Si MOSFET is connected in series as a cascade structure to drive the GaN HEMT as given in Fig. 3. This structure shifts the safety driving border.

The turn-on/off principle of cascade GaN HEMT is absolutely simple. During the turn-on period, Si MOSFET turns on first. Therefore, the source-to-gate voltage of GaN HEMT decreases. This causes the GaN device to turn on after the gate-source voltage reaches the threshold voltage. In the same manner, during the turn-off period, the MOSFET turns off initially, the gate-source voltage falls below the threshold limit, and the device turns off. On or off state of GaN HEMT can be controlled by changing the on/off state of low-voltage Si MOSFET. This cascade structure makes switching devices compatible with commercial MOSFET or IGBT drivers [15-18].

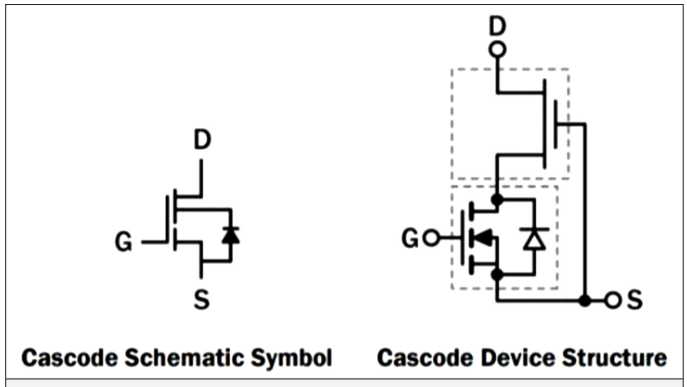

Fig. 3. The cascaded device structure, the GaN is normally-off.

B. Analytical Power Loss Calculations of GaN Devices

In hard-switching applications, the reverse recovery effect of the body diode greatly increases the switching loss on the diode, and therefore reverse recovery loss limits the switching frequency. Reverse recovery charge Q_{rr} causes more switching loss, especially at high frequencies [20]. GaN devices offer improved efficiency over silicon ones, through their lower gate charge, crossover loss, and reverse recovery charge. Since the reverse recovery charge is very low, Q_{rr} losses can be neglected in rough calculations. Nevertheless, a small parasitic capacitance related to output charge Q_{oss} can still be found during hard-switching commutation [21].

The GaN switch losses are calculated numerically by using (1)–(8), where P_{off} is turn-off loss, $P_{overlap}$ is overlap loss, P_{gate} is gate loss, P_{Qoss}, output charge loss, $P_{death-time}$, deadtime loss, P_{cond}, conduction loss, R_g, internal gate resistance, R_{gext}, external resistance, C_{iss}, effective input capacitance, V_{plt}, gate plateau voltage, V_{sd}, reverse voltage, V_{th}, threshold voltage, $R_{ds(ON)}$, drain-source on state resistance, $V_{g-recom}$, on-state gate voltage, $t_{f-current}$, turn-off time period, $t_{r-voltage}$, turn-on time period, V_d and I_d, voltage and rms current of switch, respectively. t_d is death time, t_{fall1}, t_{fall2}, and t_{rise1} are overlap times of voltage and current of GaN.

This paper aims to provide a comprehensive explanation of the loss model for GaN switches, focusing on various power loss components associated with their operation. By considering turn-off loss, overlap loss, gate loss, output charge loss, deadtime loss, conduction loss, gate resistance, effective input capacitance, and other relevant parameters, a detailed analysis of power dissipation can be achieved. Through the utilization of numerical equations, this loss model enables accurate evaluation and analysis of power losses in GaN switches, providing valuable insights into the performance and efficiency of GaN-based microinverters.

Efficiency and performance of GaN-based microinverters are directly influenced by power losses occurring in GaN switches. Therefore, it is essential to develop a detailed loss model that encompasses all relevant factors impacting power dissipation. This study addresses this need by offering an in-depth explanation of the loss model for GaN switches, encompassing a comprehensive analysis of different loss components [22].

All in all, the presented loss model provides a thorough understanding of power losses in GaN switches. By considering turn-off loss, overlap loss, gate loss, output charge loss, deadtime loss, conduction loss, gate resistance, and effective input capacitance, it allows for a detailed analysis of power dissipation. This loss model serves as a valuable tool for evaluating the performance and efficiency of GaN-based microinverters, facilitating the optimization of their design and operation.

$$P_{off} = V_d \cdot I_d \cdot (t_{f-current} + t_{r-voltage}) \cdot 0.5 \cdot f_{sw} \quad (1)$$

$$t_{f-current} = (R_g + R_{gext}) \cdot C_{iss} \cdot \log(\frac{V_{plt}}{V_{th}}) \quad (2)$$

$$t_{r-voltage} = (R_g + R_{gext}) \cdot C_{iss} \cdot \frac{V_d}{V_{plt}} \quad (3)$$

$$P_{overlap} = V_d \cdot I_d \cdot f_{sw} \cdot (t_{fall1} + t_{rise1} + t_{fall2}) \cdot 0.5 \quad (4)$$

$$P_{gate} = Q_g \cdot V_{g-recom} \cdot f_{sw} \quad (5)$$

$$P_{Q_{oss}} = Q_{oss} \cdot V_d \cdot f_{sw} \quad (6)$$

$$P_{dead-time} = I_d \cdot V_{sd} \cdot t_d \cdot f_{sw} \quad (7)$$

$$P_{cond} = R_{ds(ON)} \cdot (I_d)^2 \quad (8)$$

III. STRUCTURE AND OPERATING PRINCIPLES OF MICRO-INVERTER TECHNOLOGY

Solar micro-inverters are composed of two stages. The first stage includes any kind of DC–DC converter while the second stage includes the full-bridge inverter as given in Fig. 4.

Switching devices of DC–DC converter are controlled by a closed loop control system where an MPPT algorithm determines the needed duty ratios. Single-phase full-bridge inverters have four switching devices and they are controlled by SPWM with a PI controller. The L, LC, and LCL filters can be connected to the output of the inverter in order to reduce harmonic contents.

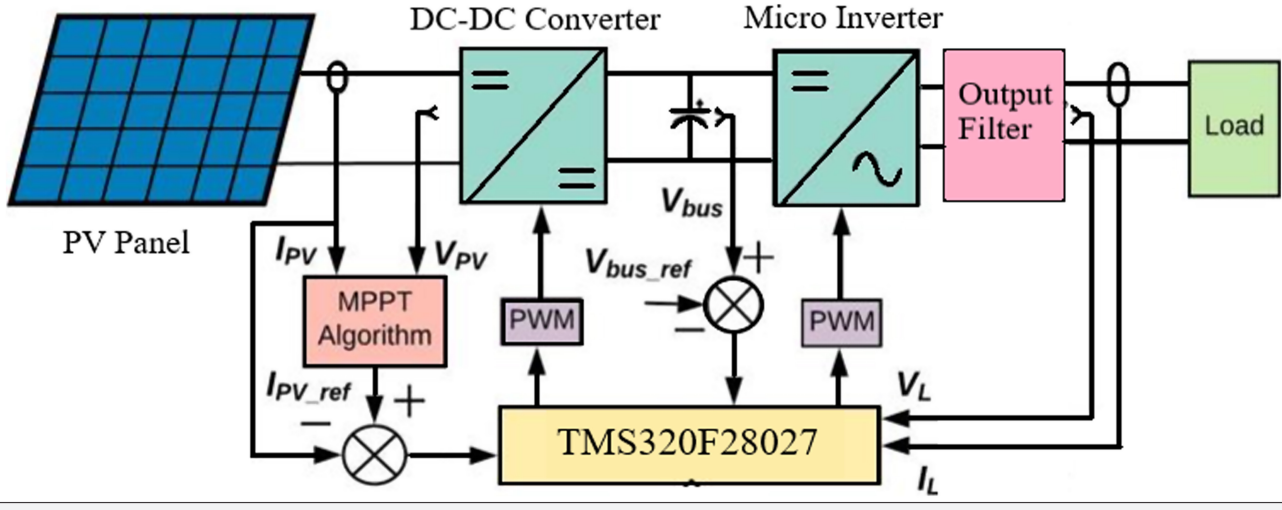

Fig. 4. Typical structure of a solar micro-inverter.

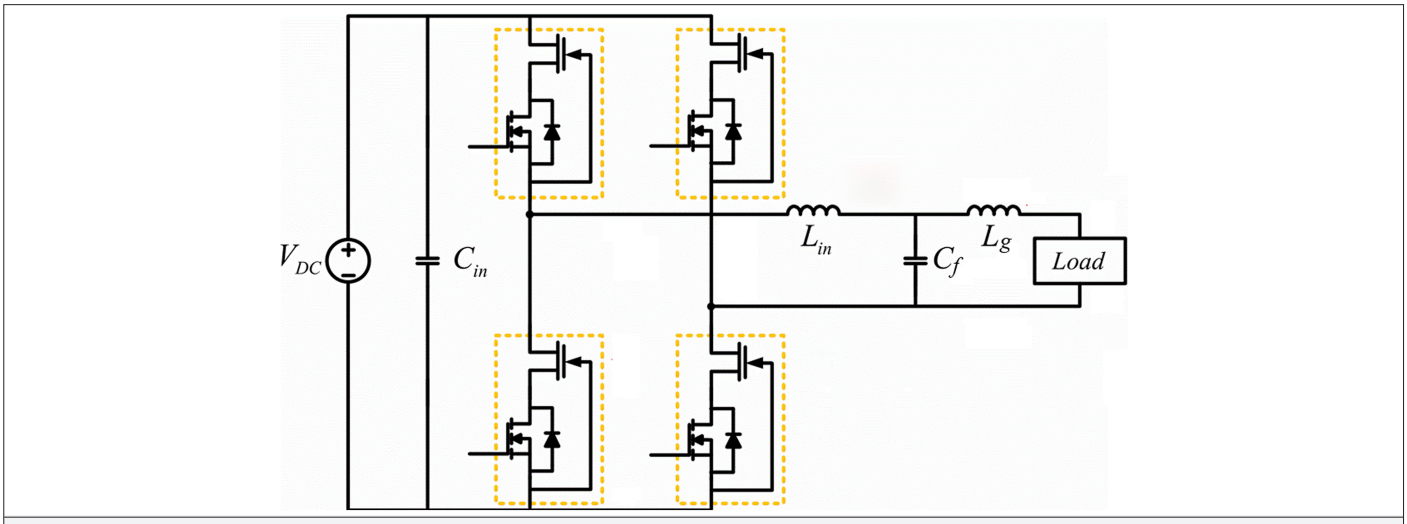

Fig. 5. Full bridge inverter topology with GaN HEMTs [22]. GaN, gallium nitride; HEMTs, high-electron-mobility transistors.

A. Single-Phase Full-Bridge Inverter

The full-bridge inverter topology converts the applied DC input voltage into a non-sinusoidal alternating voltage at the output. A single-phase full-bridge inverter built with four cascade GaN HEMTs is illustrated in Fig. 5 [23]. The GaN HEMT pairs conduct in turn one by one. The two output terminals are connected to the center points of either leg of the full-bridge circuit.

B. SPWM Technique

The output voltage waveform of an inverter is determined by the switching technique and switching frequency. Various SPWM techniques are used in single-phase inverter applications in order to obtain an output voltage with the lowest harmonic content. SPWM is a popular control method widely used in power electronic inverters.

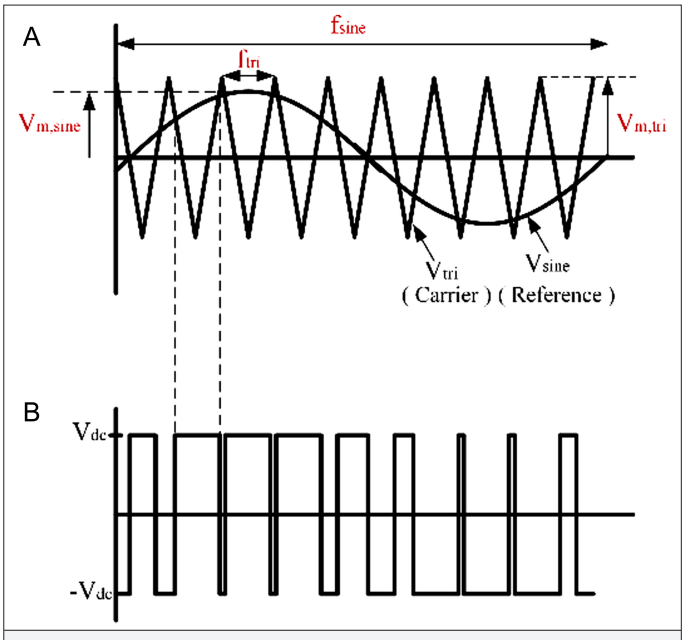

Fig. 6. Bipolar switching scheme: (a) reference and carrier signal and (b) output voltage of inverter.

It has advantages like low switching losses, the output has less harmonic and the method itself is easy to implement [24, 25].

Bipolar and unipolar switching methods are the most familiar methods to obtain SPWM signals in the literature. In SPWM techniques, a sinusoidal reference signal (v_{sine}), namely modulating or control signal, is needed for the control of power switches on each leg and a triangular wave (v_{tri}) controlling switching frequency is required [25].

In bipolar switching, a sample sinusoidal reference signal and a triangular carrier signal are illustrated in Fig. 6(A) together with their characteristic values and Fig. 6(B) indicates the change of output voltage accordingly. When the instantaneous value of the reference sinusoidal signal is greater than that of the carrier wave, the output voltage is equal to the dc bus voltage and when it is less, the output voltage is equal to the inverse of the dc bus voltage.

The ratio of the peak value of the reference wave to the peak value of the triangular carrier wave is called the modulation index, M_a. The modulation index changes the amplitude of the output voltage fundamental harmonic. The ratio of the triangular carrier wave frequency (f_{tri}) to the reference wave frequency (f_{sine}) is the frequency modulation ratio, m_f. The larger the m_f the more harmonic components are to be removed from the inverter output [23-25].

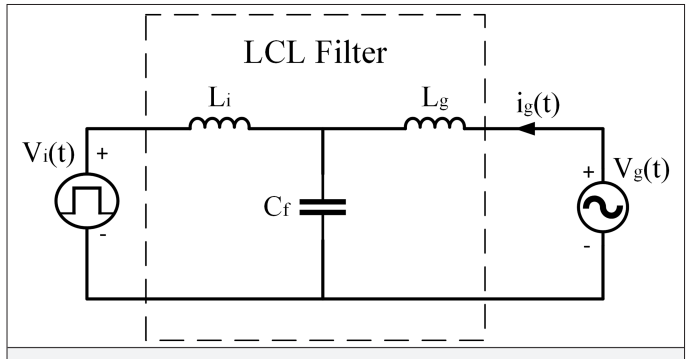

Fig. 7. Basic circuit topology of LCL filter.

$$M_a = \frac{V_{sine}}{V_{tri}} \quad (9)$$

$$m_f = \frac{f_{tri}}{f_{sine}} \quad (10)$$

C. LCL Filter

It is necessary to filter harmonics remaining after the modulation stage, especially of a grid-connected voltage-source inverter [26]. Therefore, in the literature, L, LC, and LCL filters are used to reduce the harmonic contents of inverter output Fig. 6.

L-type filter negatively affects the dynamics of the system by causing a voltage drop due to its late response time. A parallel capacitor with low reactance and high impedance at a high switching frequency is added to enable the L filter to reduce harmonics better. In an LC filter, the capacitor value is higher in order to reduce losses and costs. But large capacitor values result in high inrush current and resonance problems. Later, LCL filters were started to be used to eliminate these disadvantages. They provide better coupling with the network while serving a better harmonic reduction feature with small inductance and capacitance values. The resonance effect that may occur in an LCL filter can be eliminated with a series resistance. However, LCL filters have several drawbacks such as the filter's total impedance and increased capacitor reactive power consumption [27]. The basic circuit topology of an LCL filter is given in Fig. 7

TABLE II. OPERATIONAL VALUES OF MICRO-INVERTER AND LCL FILTER

V_{out} = 80 V (RMS)	P_{out} = 250 W	V_{in} = 113 V
f_{grid} = 50 Hz	f_{sw} = 50 kHz	I_{in} = 2.2 A

representing inverter-side and grid (load)-side inductances (L_i and L_g, respectively).

Different quantities, such as current ripple, filter size, and switching ripple attenuation, have to be considered in designing an LCL filter, and the value of line-to-line RMS inverter output voltage (V_{out}), rated active power of inverter output (P_{out}), DC link voltage (V_{in}), grid frequency (f_{grid}), and switching frequency (f_{sw}) are necessary for calculation.

The paper highlights the advantages of incorporating an LCL filter with microinverters. The inclusion of an LCL filter allows for the reduction of harmonic content and improvement of the output waveform quality. This results in the attenuation of high-frequency harmonics, leading to a cleaner and more sinusoidal output waveform. Consequently, distortion is reduced, and system performance is enhanced. Additionally, efficient power transfer and system stability are achieved by striking a balance between harmonic attenuation and desired power transmission. The integration of an LCL filter ensures compliance with grid interconnection requirements, facilitating seamless integration with the grid.

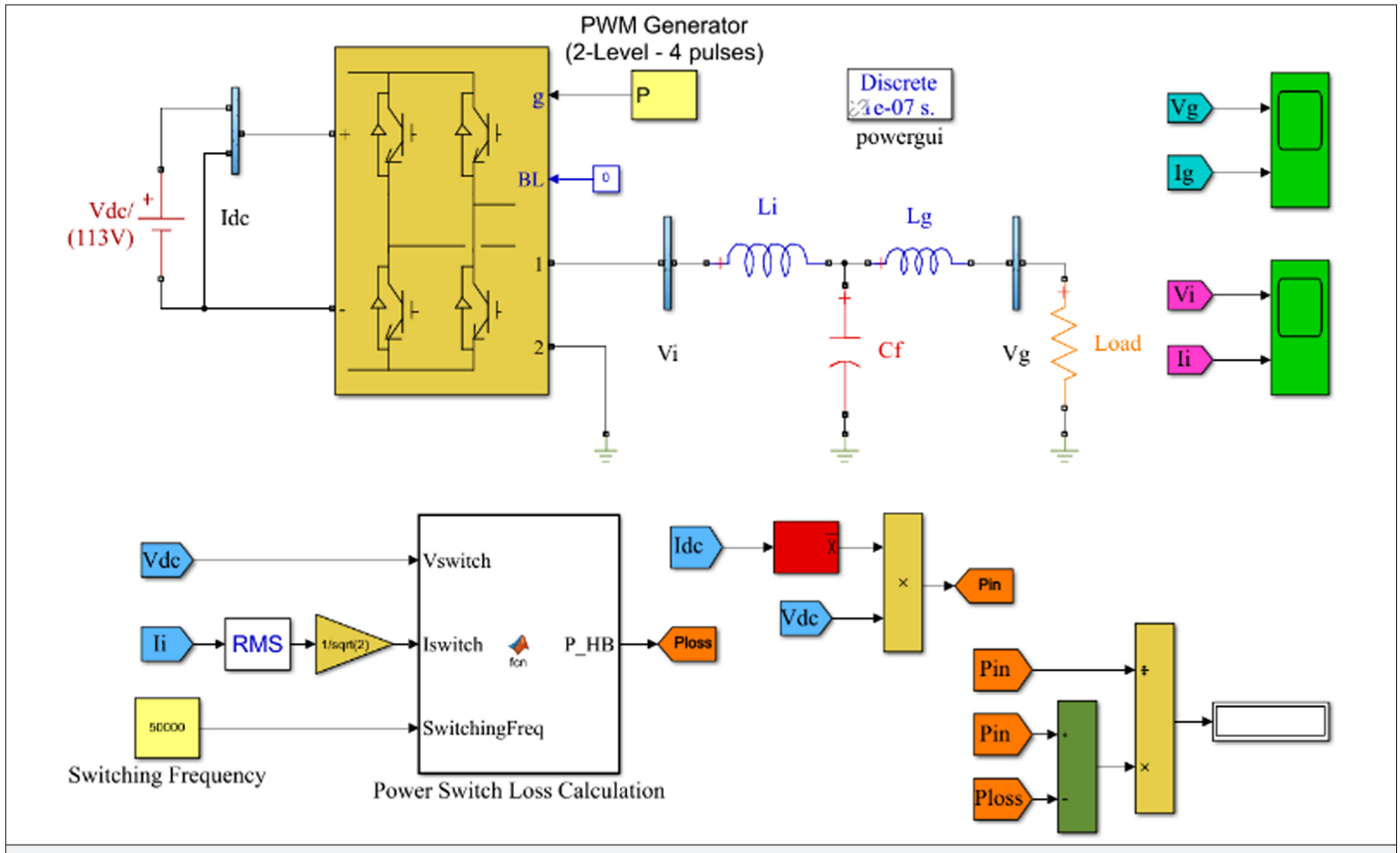

Fig. 8. Simulation setup of the designed micro-inverter.

IV. INVERTER DESIGN

Here in this study, the bipolar SPWM technique was used to minimize the harmonic content. The design parameters for the LCL filter of the micro-inverter are given in Table II.

A. Filter Design

First, the base values of impedance (Z_b) and base capacitance (C_b) of the filter were calculated as in (11) and (12) [28].

$$Z_b = \frac{V_{out}^2}{P_{out}} = 25.6\Omega \tag{11}$$

$$C_b = \frac{1}{w \cdot Z_b} = 124.3\mu F \tag{12}$$

After the determination of base components, the inverter side inductance (L_i) limiting the maximum output current ripple (ΔI_{Lmax}) by 10% of the rated current amplitude was calculated accordingly in (13) and (14).

$$\Delta I_{L\max} = 0.1 \cdot \frac{P_{out}\sqrt{2}}{V_{out}} = 0.442A \tag{13}$$

$$L_i = \frac{V_{in}}{16 \cdot f_{sw} \cdot \Delta I_{L\max}} = 319\mu H \tag{14}$$

TABLE III. COMMON IMPORTANT PARAMETERS FOR SWITCHES USED IN SIMULATION

Parameters	Abbreviation	Value
DC bus voltage	V_d	113 V
Switching frequency	f_{sw}	50 kHz and 100 kHz
DC bus current	I_{in}	2.2 A
Filter input inductance	L_i	319 µH
Filter output inductance	L_g	191 µH
Filter capacitance	C_f	..F
Effective input capacitance	C_{iss}	1130 pF
RMS current in switch	I_d	2.474 A
Reverse voltage	V_{sd}	1.5 V
Turn-off time period	$t_{f-current}$	5 ns
Turn-on time period	$t_{r-voltage}$	7.5 ns
Threshold voltage	V_{th}	2.1 V
On-state gate voltage	$V_{g-recom}$	9 V
Drain-source on state resistance	$R_{ds(ON)}$	72 mW
Dead time	t_d	50 ns
Gate charge	Q_g	14.6 nC
Reverse recovery charge	Q_{rr}	90 nC

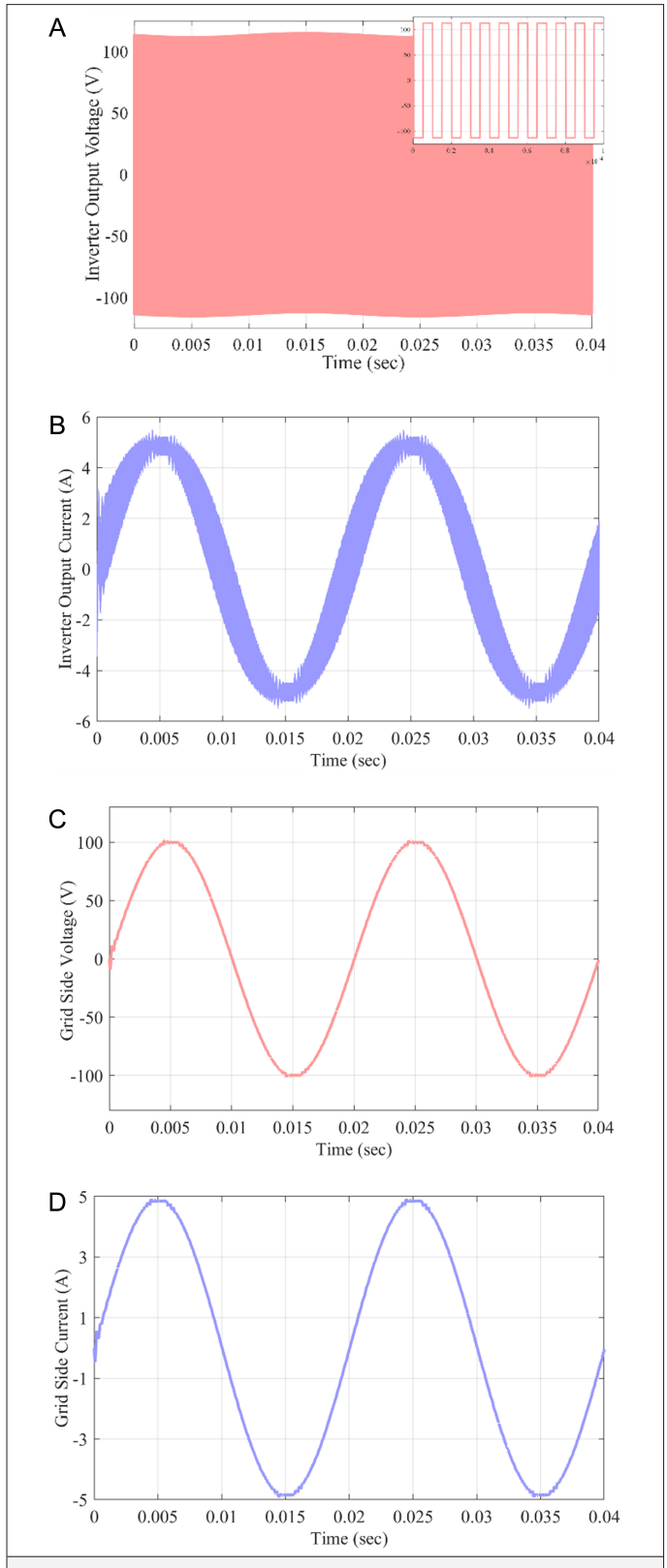

Fig. 9. Simulation results at 50 kHz switching frequency: (A) inverter output voltage (V_i), (B) inverter output current (I_i), (C) grid side voltage (V_g), and (D) grid side current (I_g).

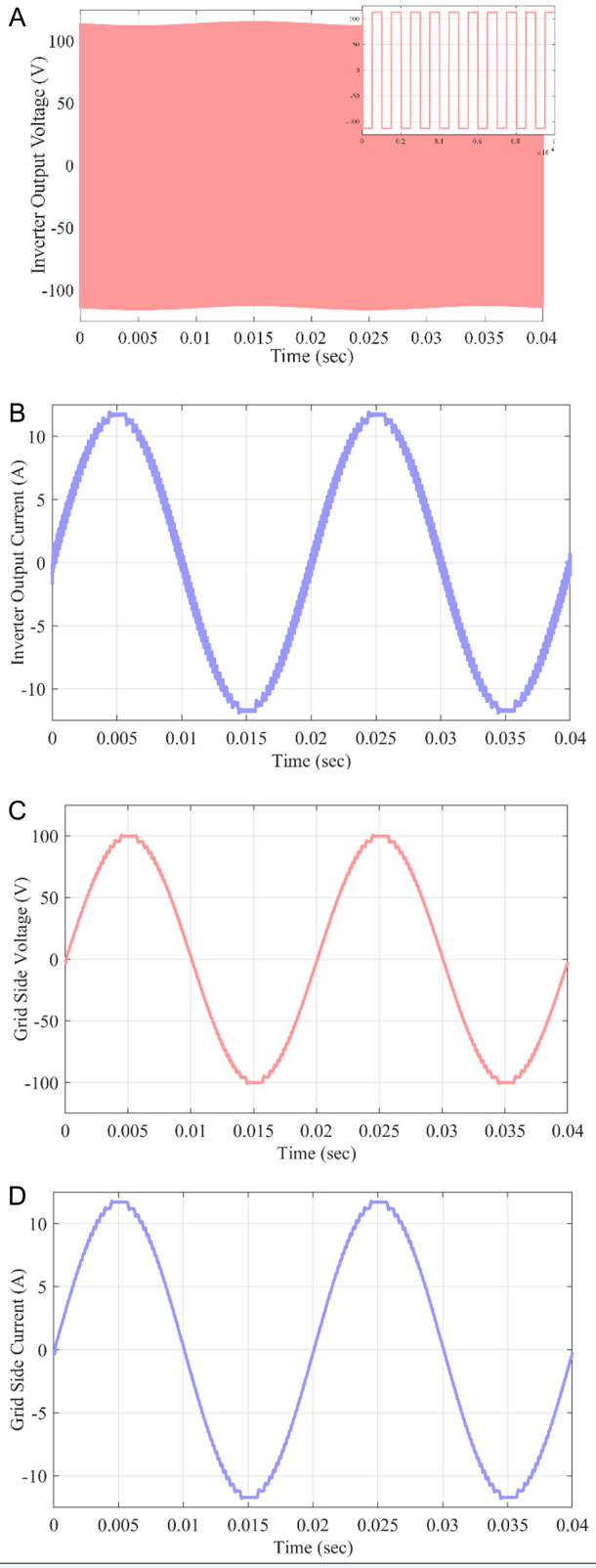

Fig. 10. Simulation results at 100 kHz switching frequency: (a) inverter output voltage (V_i), (b) inverter output current (I_i), (c) grid side voltage (V_g), and (d) Grid side current (I_g).

TABLE IV. THD COMPARISON OF INVERTER OUTPUT AND GRID SIDE VOLTAGE-CURRENT FOR DIFFERENT SWITCHING FREQUENCIES

THD (%)	50 kHz	100 kHz
V_i	85.38	85.04
I_i	17.88	10.58
V_g	1.02	1.96
I_g	1.02	1.96

Since the maximum power factor variation acceptable by the grid is 5% [28], filter capacity (C_f) can be calculated as in (15).

$$C_f = 0.05 \cdot C_b = 6.2\mu F \tag{15}$$

The grid side inductance (L_g) can be calculated as in (16) in a practical way [28].

$$L_g = 0.6 \cdot L_i = 191\mu H \tag{16}$$

The transfer function of the LCL filter can be obtained by assuming that the grid-side voltage source is an ideal voltage source capable of damping all harmonic frequencies. The transfer function of the LCL filter with the assumption that "$V_g = 0$" is given in (17).

$$\frac{i_g}{v_i} = \frac{1}{L_i \cdot C_f \cdot L_g \cdot s^3 + (L_i + L_g) \cdot s} \tag{17}$$

B. Simulation Study

In this part of the study, the mathematical model of the designed 250 W micro-inverter with the given designed output filter and the power loss calculation model of GaN HEMTs were both simulated in MATLAB/Simulink at different switching frequencies. The simulation setup of the designed micro-inverter can be seen in Fig. 8.

Analytical loss formulations given in (1)–(8) were implemented in the MATLAB/Simulink model for the analytical calculation of the losses of GaN HEMTs. In Table III, all common important parameters for switches used in the simulation are given.

Simulation results for 50 kHz and 100 kHz switching frequencies for the inverter output and the grid side quantities were obtained and are given in Fig. 9 and Fig. 10, respectively. The total harmonic distortions (THD) of all measured currents and voltages are all given in Table IV.

It can be seen that the THD of the current and voltage at the inverter output decreases with the increasing switching frequency, while there is a slight increase in the harmonic distortion of the current and voltage on the grid side where the effect of the LCL filter at the inverter output on the THD can be observed.

For detailed in-depth analysis, the analytically calculated power losses of GaN HEMTs calculated in the simulation are given in Fig. 11 as a radar chart in comparison for both 50 kHz and 100 kHz switching frequencies in order to observe the distribution of Gan HEMTs power losses.

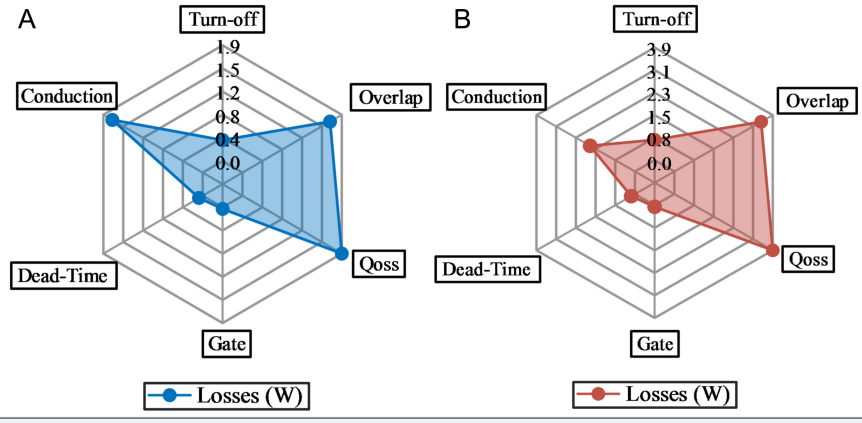

Fig. 11. Analytical power losses of GaN HEMT at (A)50 kHz and (B)100 kHz switching frequency. GaN, gallium nitride; HEMT, high-electron-mobility transistor.

V. PRACTICAL STAGE AND EXPERIMENTAL EVALUATION

A. Selection of Power Switch and Gate Drive Circuit

In this study, TPH3212PS GaN switches and ADuM4223 half-bridge gate drivers were used for the power stage of the micro-inverter. The TPH3212PS GaN HEMT has a 650 V drain to source voltage and 72 *m*Ω on-state resistance. Besides, it is a normally-off device which combines state-of-the-art high-voltage GaN HEMT and low-voltage Si MOSFET technologies.

Each ADuM4223 half-bridge gate drivers provide two independent isolated channels. They operate at an input supply range of 3.0–5.5 V, providing compatibility with lower voltage systems. ADuM4223 can be operated at a maximum frequency of 1 MHz and in the range of 4.5–18 V supply voltage.

B. Filter Inductances and Capacitance

Toroidal cores with inductance factor *AL* of 12 600 *nH/Turn*^{2} were selected for calculated LCL filter inductances. The number of turns for each inductance can be calculated with a simple equation given in (18) [29].

$$AL = \frac{L}{N^2} \tag{18}$$

According to (18), four turns are sufficient for an inductance of 198 µH, while six turns are sufficient for 319 µH. DUCATI 475V/6 µF film capacitor was selected for filter capacitance.

C. Design Layout

The performance of GaN HEMT devices used at high switching frequency can be easily affected by the interference on the PCB layout. The effects of these parasites were modeled and their effects were investigated in detail in [23-[26]]. In order to minimize the interference problems caused by parasitic inductances, it is necessary to keep the high-frequency power loop inductance as low as possible. In order to make the inductance of the path between the gate driver and the gate terminal as small as possible, the gate drivers have to be placed very close to the GaN HEMTs. The gate control signal paths can be placed at the top layer of the PCB. All elements around the gate driver should be placed on the same side, and connections (via) that increase the parasitic inductance to the substrate should be avoided. In order to reduce the capacitance between the switching node and the ground supply, the distance between them should be as small as possible.

A 40 µF/400 V film capacitor is added to the DC bus to smooth the input voltage. The side view of the designed and prototyped micro-inverter is given in Fig. 12.

D. Experimental Results

Fig. 13 shows the experimental setup for the designed 250-W high-efficient micro-inverter prototype.

The efficiencies of the prototyped micro-inverter at different switching frequencies, different input voltages, and different operating currents were measured and compared with the values calculated from the analytical loss model. During the tests, the maximum power level is limited to 250 W rated input power. Fig. 14 and Table V show the "efficiencies vs. DC bus current" for different voltage values at 50 kHz and 100 kHz switching frequencies, respectively. The efficiency values of the rated operation point (113 V DC bus voltage and 2.2

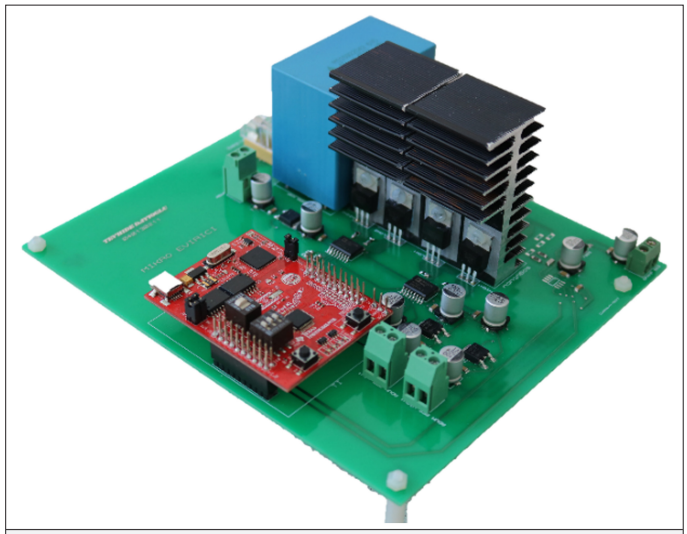

Fig. 12. Side view of a prototyped micro-inverter.

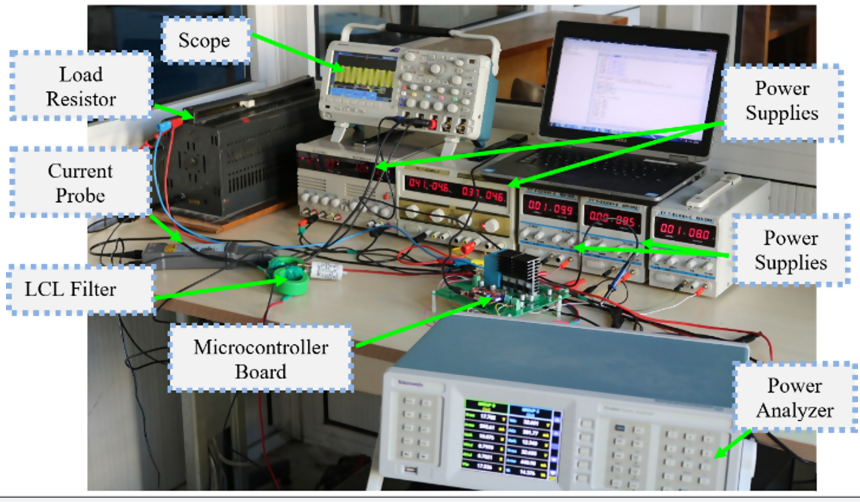

Fig. 13. Test setup of a micro-inverter.

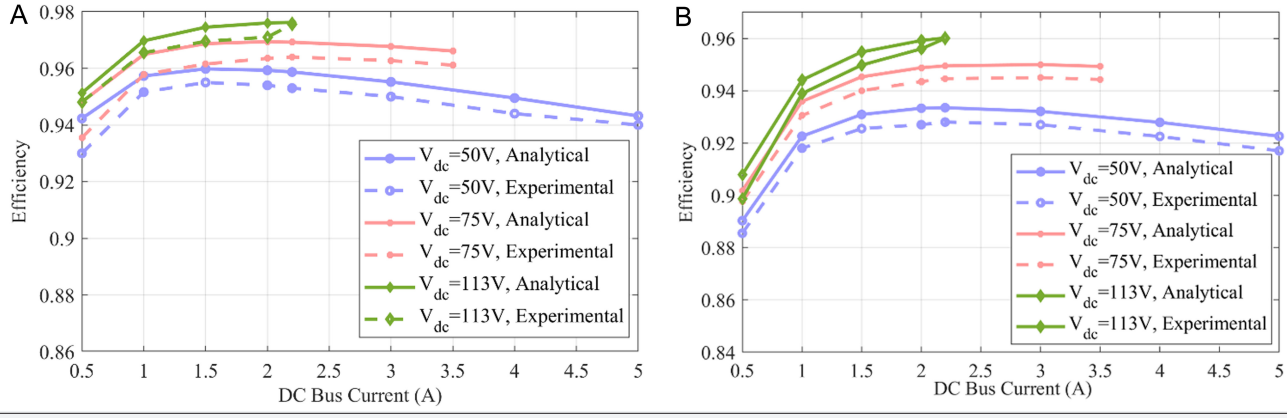

Fig. 14. Efficiencies for different voltage and current values at (A) 50 kHz and (B) 100 kHz switching frequency.

TABLE V. COMPARISON OF EFFICIENCY IN ANALYTICAL AND EXPERIMENTAL

50 kHz	**50 V**		**75 V**		**113 V**	
DC Bus Current	Analytical	Experimental	Analytical	Experimental	Analytical	Experimental
0.5	0.942	0.93	0.947	0.935	0.951	0.948
1	0.957	0.951	0.965	0.957	0.969	0.965
1.5	0.96	0.955	0.969	0.961	0.974	0.969
2	0.959	0.954	0.935	0.963	0.976	0.971
100 kHz	50 V		75 V		113 V	
DC Bus Current	Analytical	Experimental	Analytical	Experimental	Analytical	Experimental
0.5	0.89	0.885	0.901	0.897	0.908	0.899
1	0.923	0.918	0.936	0.93	0.944	0.939
1.5	0.93	0.925	0.945	0.94	0.955	0.95
2	0.933	0.927	0.948	0.943	0.96	0.956

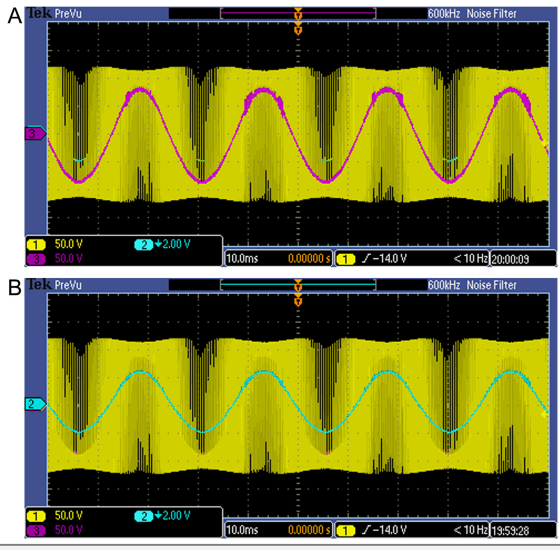

Fig. 15. Oscilloscope waveform of the micro-inverter: (A) output voltage and (B) output current with or without an LCL filter.

TABLE VI. THD COMPARISON OF INVERTER OUTPUT VOLTAGE AND CURRENT WITH AND WITHOUT LCL FILTER

	THD of Inverter Output Current (%)	THD of Inverter Output Voltage (%)
Without LCL filter	76.553	21.960
With LCL filter	1.5210	1.5162

A DC bus current) at 50 kHz and 100 kHz switching frequency were measured as 97.5% and 96%, respectively.

In order to determine the effect of the calculated LCL filter, the current and voltage scope waveforms of grid side and inverter output are given in Fig. 15. In addition, the THD of the output voltage and current with or without the LCL filter was measured and given in Table VI for the rated operated point (113 V–2.2 A).

IV. CONCLUSION

The main goal of this study is to present a detailed design methodology for a high-efficiency micro-inverter accommodating TO-220 packaged GaN-HEMT devices. The parasitic inductances of the design were minimized and an LCL filter was added to the grid side. Analytical calculations, simulation, practical implementation, and test stages are given in detail. It is a well-known fact that designing a micro-inverter with TO-220 packaged GaN-HEMT is a very difficult task at high switching frequencies since terminal inductances caused by the package make it difficult to operate at higher switching frequencies.

The effect of different switching frequencies on the grid side of the micro-inverter was also analyzed for different load levels. In order to achieve a high power density and high efficiency, the switching frequency was kept as high as possible and GaN HEMTs that can operate at high switching frequencies were used. An improved and detailed loss model for GaN HEMTs was implemented to the simulation blocks for analytical calculations in order to contribute to choosing power devices to be installed into the micro-inverters. Two different relatively high switching frequencies (50 kHz and 100 kHz) were used in the analyses and practical tests. The analytical and practical results are given in comparison to emphasize the success of the switching model, the impact of high operational frequencies and the effect of the LCL filter design. The rated values of the prototype inverter are 250 W, 113 V (DC bus voltage) and 2.2 A (DC bus current). Considerable attention was paid to PCB Layout to limit and omit the parasitic effects that may occur at the chosen high frequencies. The effect of the filter was determined for the two mentioned high switching frequencies and it was shown that THD of the output voltage and current for both frequencies were reduced to acceptable levels by means of the designed LCL filter.

The designed and prototyped micro-inverter was tested practically at different operating points at 50 kHz and 100 kHz switching frequency levels and the results are given in comparison. The efficiencies of 50 kHz and 100 kHz switching frequencies for the rated operation were measured as 97.5% and 96%, respectively.

All-in-all, the design methodology for a high-power density, high-efficiency inverter including an LCL filter was introduced together with a practical study. No attention is paid to DC–DC converters connected between micro-inverters and solar panels.

Peer-review: Externally peer-reviewed.

Author Contributions: Concept – M.O.G.; Design – T.D., M.O.G.; Supervision – M.O.G., D.A.K.; Funding – T.D.; Materials – T.D., M.O.G.; Data Collection and/or Processing – T.D., M.O.G., A.L.; Analysis and/or Interpretation – T.D., M.O.G., A.L.; Literature Review – T.D., A.L.; Writing – T.D., M.O.G., A.L.; Critical Review – D.A.K., M.O.G.

Declaration of Interests: The authors have no conflicts of interest to declare.

Funding: The authors declared that this study has received no financial support.

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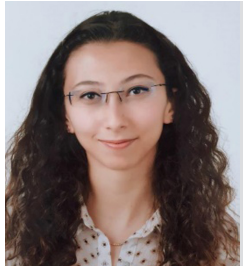

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