İSTANBUL UNIVERSITY CERRAHPAŞA

ORIGINAL ARTICLE
Electrica 2024; 24(2): 463-476

An Improved Current Ripples Minimization Technique for Cascaded DC–DC Converter in DC Microgrid

Khadidja Khattab[1], Ahmed Safa[1], Abdelmadjid Gouichiche[1], Youcef Messlem[1], Djaffar Ould Abdeslam[2], Abdelilah Chibani[1]

[1]Laboratoire de Génie Electrique et des Plasmas (LGEP), University of Tiaret, Tiaret, Algeria
[2]Laboratoire IRIMAS, University of Haute Alsace, Mulhouse, France

Cite this article as: K. Khattab, A. Safa, A. Gouichiche, Y. Messlem, D. Ould Abdeslam and A. Chibani, "An improved current ripples minimization technique for cascaded DC–DC converter in DC microgrid," *Electrica*, 24(2), 463-476, 2024.

ABSTRACT

The distributed direct current (DC) power system relies heavily on the cascaded DC–DC converter that employs a common bus to connect multiple DC–DC converters. The first stage of the cascaded DC–DC converter is responsible for injecting power from a renewable source or a battery into the DC bus. Conversely, the second stage connects a load to the DC bus, creating a constant power load (CPL) that consumes constant power regardless of the supply voltage. This behavior often causes disturbances and instabilities, leading to unwanted oscillations that adversely impact the quality of the input current. To address this issue, this paper proposes an active current ripple-damping technique that extracts the fundamental of the inductor current. When combined with the super-twisting sliding mode control, this approach effectively mitigates input current ripples and enhances the stability of the CPL. The key to this approach is the sliding surface selection, which requires a cleaned inductor current from the second boost converter. Experimental results are provided to demonstrate the effectiveness of the proposed method.
***Index Terms*—**Cascaded boost converter, constant power load (CPL), DC microgrid, harmonic extraction, inductor current ripple, modified super twisting controller.

Corresponding author:
Khadidja Khattab

E-mail:
Khadidja.khattab@univ-tiaret.dz

Received: November 26, 2023

Revision Requested: January 22, 2024

Last Revision Received: March 13, 2024

Accepted: April 12, 2024

Publication Date: May 20, 2024

DOI: 10.5152/electrica.2024.23177

I. INTRODUCTION

Due to the depletion of fossil fuel reserves and the availability of cleaner energy, the use of distributed generators has grown [1]. Consideration of distributed resources (DR) and related loads as a miniature electrical system known as a microgrid is one way to maximize the growth potential of DR [2, 3]. Microgrids have both alternate current (AC) and direct current (DC) distribution lines [4]. However, recent research has shown that the reliability and efficiency of power systems are improved by using DC distribution in microgrid systems [5]. Therefore, a DC microgrid, as shown in Fig. 1, is the best solution for a variety of reasons. Firstly, it allows the integration of renewable energy sources, which decreases environmental CO_2 emissions [5]. Additionally, DC microgrids provide high system efficiency, low cost, and simple control [6]. Moreover, in the context of modern electronic loads such as computers and servers in data centers, which necessitate DC power, DC microgrids prove highly compatible. Furthermore, even common AC loads like induction motors can be adapted into DC loads through the utilization of variable-speed drives [7]. However, unstable power loads caused by interconnecting power electronic converters in DC microgrids are a major issue. Constant power load (CPL)'s negative impedance characteristic can affect system performance [8–11]. A CPL is defined as a load that consumes a constant amount of power regardless of the supply voltage.

A CPL can appear in one of the four following cascaded configurations to affect system performance [9]:

- A strictly controlled DC/DC voltage regulator with an upstream DC/DC converter.
- A strictly controlled DC/DC voltage regulator with an input LC filter.
- A strictly controlled inverter with an upstream DC/DC converter.
- A strictly controlled inverter with an input LC filter.

A typical DC microgrid is shown in Fig. 1. In this figure, the cascading DC–DC converter topology plays a pivotal role in the DC-distributed power system [12], connecting multiple converters via

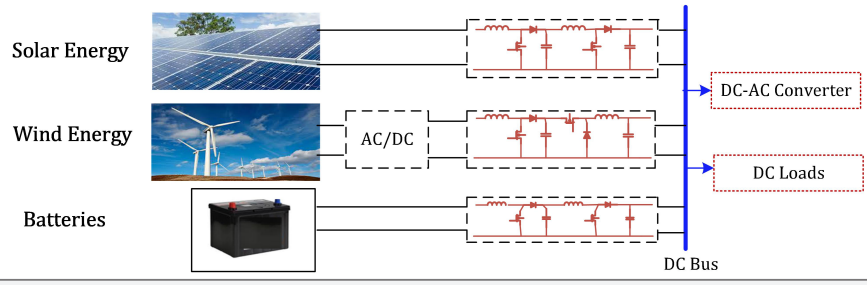

Fig. 1. Sturcture of a DC microgrid.

a common bus. This topology offers several advantages. Firstly, it has higher reliability with standardization, maintenance, expansion, and hot plug facilities [13]. Additionally, within a cascaded power system, each interconnection generates an intermediate bus voltage [13]. Furthermore, in the wind system, the DC bus voltage may be lower than the input voltage of the power factor converter; therefore, it is necessary to decrease the voltage using a second buck converter [14, 15].

A new technique has been proposed in [16] for controlling both uniform and non-uniform DC–DC systems that are connected in parallel. This fully decentralized controller uses a gradient descent technique to minimize the fundamental switching harmonic in the current and voltage ripple. The algorithm is implemented in each converter by adjusting the PWM (Pulse Width Modulation) phase shift based on the local terminal voltage sampled at each switching cycle. One major advantage of this approach is its simplified digital implementation that does not require complex optimization algorithms, look-up tables, high-fidelity detection, or oversampling measurements. However, it is important to note that the use of sensors in this method may be costly, especially if they are highly precise or specialized.

The adaptive decentralized backstepping control (DABC) of cascaded DC–DC boost converters is examined in the presence of load and voltage uncertainties and interactions between converters in [17]. The Legendre polynomials (LP) used to estimate the uncertainties and interactions adaptively have been shown to approximate them very well due to their universal approximation property. Furthermore, it is demonstrated that the proposed control strategy is robust and has a low computational burden. However, this work's control of the cascaded converters is a bit more complex.

Another work has proposed an active damping control method for a DC marine microgrid's constant power cascade system. This method involves utilizing a virtual RC feed forward loop, which effectively eliminates resonance and promotes system stability. However, implementing a virtual capacitor component may reduce dynamic characteristics and extend tuning time. As such, further research is necessary to attain optimal control of the system [18].

The use of two boost converters in cascade results in an increase in the ripples of the inductor current of the load converter. To improve the quality of the current, it is necessary to attenuate the ripples. Various control techniques have been proposed for a DC microgrid power quality using a cascaded converter, including active and passive damping techniques, as well as new converter topologies [8].

Active damping techniques have superiority over passive ones in terms of power dissipation. In [19], R. Stala and alothers analyzed the effect of phase shift between duty cycles of two-stage cascaded converters and found that a proper adjustment in the phase shift can reduce the RMS (Root Mean Square) current ripple of the capacitor without affecting the normal converter operation or requiring additional sensing circuits. Besides, it leads to an overall efficiency improvement. However, the control flowchart used to regulate the phase shift between the duty cycles of the two power-stage converter switches can be complex.

The need to boost the DC voltage generated by PV (PhotoVoltaic) arrays for grid integration, especially when only a small amount of energy is produced, is discussed in [20]. While MPPT (Maximum Power Point Tracker) converters optimize power output, they do not rectify voltage. The study introduces a switched-inductor, switched-capacitor-based DC–DC power boost converter, achieving voltage boosts of 6 to 18 times with duty ratios of 0.5 and 0.8, respectively. Cascading more switched capacitor cells doubles voltage with fewer current variations. The converter employs only two power switches, simplifying control mechanisms. Simulation shows over 98% efficiency, while experimental results indicate close to 96%. It is noted that larger power values yield better efficiency. The converter suits portable lighting, off-grid, and micro-grid PV applications, with the potential for high-power use via appropriate semiconductor devices and inductors.

In this paper, a novel active damping technique is proposed. In this technique, the fast Fourier transformer is used to extract the inductor current's fundamental frequency, which is then multiplied by a weighted gain and subtracted from the raw current to produce a filtered current. This filtered current is then used in the modified super-twisting control's sliding surface instead of the inductor current itself. This technique eliminates the need for additional sensors or complicated control systems. The mathematical model of the proposed approach is explained in detail, followed by an experimental testbed that demonstrates its effectiveness. This technique offers a highly promising solution to improve the performance and stability of two-stage DC–DC converters.

The paper is organized as follows: A DC microgrid consisting of two cascaded DC–DC boost converters is modeled with a state space representation in Section II. Section III describes the extraction method of the fundamental harmonic of the input current of the CPL to use in the proposed technique in this work. The modified super twisting control is described in section IV. An analysis of the stability of the modified super-twisting controller is presented in section V. The experiments verify the effectiveness of the suggested technique in

Section VI; three tests are performed to check the effect of the proposed approach on the inductor current ripple and the impact of changing the gain G and the load resistance. Finally, Section VII concludes this paper.

II. SYSTEM DESCRIPTION

This study focuses on mitigating the input current ripple in a cascaded DC–DC converter. The system under study is illustrated in Fig. 2. The system has two conventional DC–DC boosts; the one connected to the DC power source is named the source converter, and the other is the load converter. The two converters are controlled separately and have different switching frequencies.

A. State Space Model of the Cascaded Boost Converter

The state-space model of the cascading boost converters is presented in this sub-section to describe the functionality of both converters and the various variable names used in the following sections [21]:

$$x_1 = -\frac{(1-u_1).V_{out1}}{L_1} + \frac{V_{in1}}{L_1} \quad (1)$$

$$x_2 = \frac{(1-u_1).I_{L1}}{C_1} - \frac{I_{L2}}{C_1} \quad (2)$$

$$x_3 = -\frac{(1-u_2).V_{out2}}{L_2} + \frac{V_{out1}}{L_2} \quad (3)$$

$$x_4 = \frac{(1-u_2).I_{L2}}{C_2} - \frac{V_{out2}}{C_2 R_2} \quad (4)$$

With $x_1 = I_{L1}$; $x_2 = V_{out1}$; $x_3 = I_{L2}$ and $x_4 = V_{out2}$.

B. Control Design of the Power Converter

To enhance the generality of our study, a conventional cascaded proportional-integral (PI) controller is employed for the first chopper, as shown in Fig. 3. Implementing a cascaded PI controller enables a more secure and reliable performance of the boost converter. The transfer function from the control input to the power converter output is expressed in the following form [22]:

$$G_{b1}(s) = \frac{G_{d0}.(1 - s.\frac{1}{w_z})}{1 + s.\frac{1}{Q.w_0} + s\dagger\frac{1}{w_0^2}} \quad (5)$$

With $G_{d0} = \frac{V_{out1}}{(1-D_1)}$; $w_z = \frac{R_1}{L_1}.(1-D_1)\dagger$; $w_0 = \frac{(1-D_1)}{\sqrt{L_1.C_1}}$ and $Q = (1-D_1).R_1.\sqrt{\frac{C_1}{L_1}}$.

Where the load converter is considered as a load of the first converter named R_1.

The expressions for the PI voltage and current controllers are given respectively by equations (6) and (7)

$$G_{c1}(s) = G_{cv}.(1 + \frac{W_{Lv}}{s}) \quad (6)$$

$$G_{c2}(s) = G_{ci}.(1 + \frac{W_{Li}}{s}) \quad (7)$$

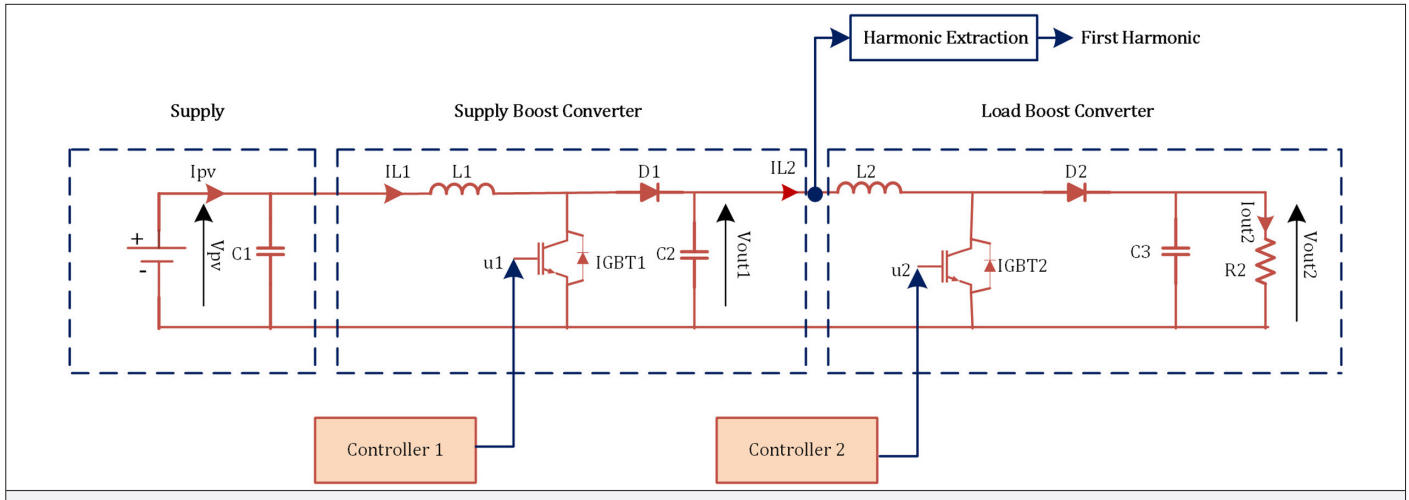

Fig. 2. Control design of the cascaded boost converter.

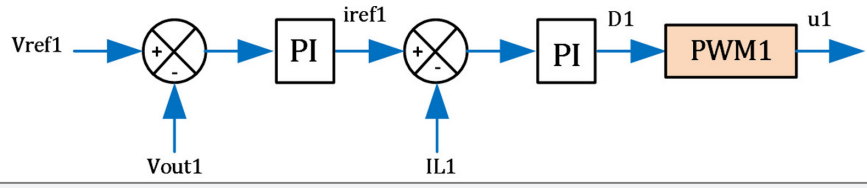

Fig. 3. Voltage and current control of the DC–DC supply converter.

With $K_{pv} = G_{cv}$; $K_{iv} = G_{cv}W_{Lv}$; $K_{pi} = G_{ci}$ and $K_{ii} = G_{ci}W_{Li}$.

The PI controller gains of the source converter are determined by a frequency analysis (Bode diagram).

C. Control Design of the Load Converter

The load side converter—which acts as a CPL—is the most fragile part of a DC microgrid. Therefore, a CPL poses a stability challenge that must be handled carefully to guarantee the stability of the whole system. Thus, in this study, we used the super-twisting controller known for its robustness.

Besides the robustness, input current ripple is the other concern in this study. Therefore, a new sliding surface is proposed for the super-twisting controller that considerably reduces the input current ripples. Furthermore, a weighted fundamental component is subtracted from the input current; this approach is detailed in the following sections. The control design of the load converter is shown in Fig. 4.

III. FUNDAMENTAL COMPONENT EXTRACTION

The input current ripples of the CPL are analyzed in terms of harmonics using a Fourier series decomposition. The inductor current is expressed as follows:

$$\begin{cases} I_{L2} = \dfrac{\Delta I_{L2}}{D_2 T_2} t + I_{\min}; 0 < t < D_2 T_2 \\ I_{L2} = \dfrac{-\Delta I_{L2}}{(1-D_2)T_2}(t - T_2) + I_{\min}; D_2 T_2 < t < T_2, \end{cases} \quad (8)$$

According to Fourier series theory, the input current (load converter inductor current or source converter output current), shown in Fig. 5, is decomposed into a DC component and a series of sine and cosine waveforms are shown as follows [23]:

$$i_{CPL}(t) = i_{out1}(t) = I_{L2}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n.cos(nwt) + b_n.sin(nwt)) \quad (9)$$

Where $w = \dfrac{2\pi}{T_2}$, T_2 is the signal period. The coefficients a_n and b_n are:

$$a_n = \frac{2}{T_2}\int_0^T i_{CPL}(t).cos(nwt)dt \quad (10)$$

$$b_n = \frac{2}{T_2}\int_0^T i_{CPL}(t).\sin(nwt)dt \quad (11)$$

Therefore, the amplitude and phase of the n^{th} harmonic component of the input current are obtained by:

$$A_n = \sqrt{a_n^2 + b_n^2} \quad (12)$$

$$A_n = \sqrt{a_n^2 + b_n^2} \quad (13)$$

The coefficients a_n and b_n are obtained as:

$$a_0 = 2I_{\min} \quad (14)$$

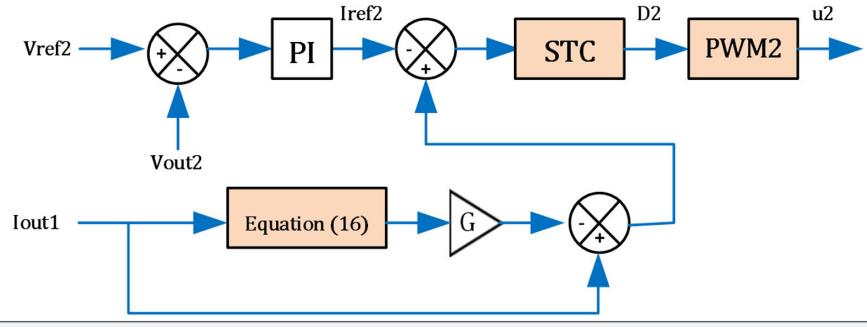

Fig. 4. Voltage and current control of the DC–DC load converter.

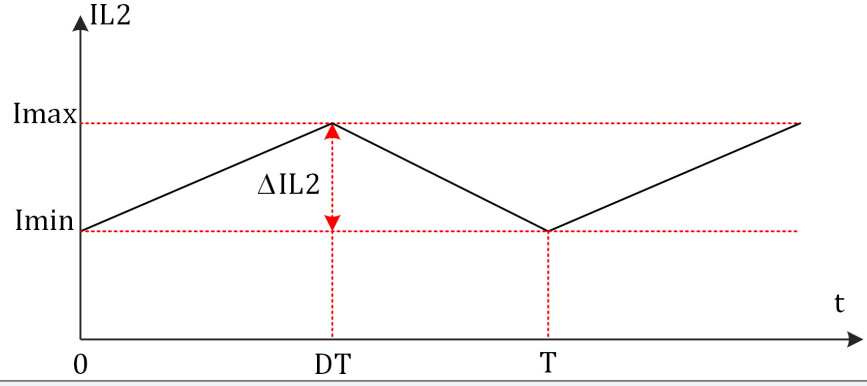

Fig. 5. Indutor current waveform of the load converter (CPL).

$$a_n = \frac{1}{D_2(1-D_2)} \frac{1}{n^2} \frac{\Delta I_{L2}}{2\pi^2} (\cos(2n\pi d) - 1); n \geq 1 \quad (15)$$

$$b_n = \frac{1}{D_2(1-D_2)} \frac{1}{n^2} \frac{\Delta I_{L2}}{2\pi^2} (\sin(2n\pi d)); n \geq 1 \quad (16)$$

The amplitude and phase of n^{th} harmonic components are obtained as follows:

$$A_n = \frac{1}{n^2\pi^2} \frac{V_{out1}}{L_2 f_{d2}} \frac{1}{(1-D_2)} \sin(n\pi D_2); n \geq 1 \quad (17)$$

$$\varphi_n = n\pi D_2 + \frac{\pi}{2} \quad (18)$$

The fundamental is extracted in the proposed control $n = 1$:

$$A_1 = \frac{1}{\pi^2} \frac{V_{out1}}{L_2 f_{d2}} \frac{1}{(1-D_2)} \sin(\pi D_2) \quad (19)$$

$$\varphi_1 = \pi D_2 + \frac{\pi}{2} \quad (20)$$

After the load DC–DC converter's inductor current has been decomposed using the Fourier series, the fundamental is multiplied by a gain and subtracted from the original current. The expression for the modified ripple-minimized current used in super-twist control is written as follows:

$$i_{sta} = i_{out1} - GA_1 \quad (21)$$

Where G is a positive gain, and A_1 is the first harmonic's module.

IV. SUPER TWISTING CONTROLLER

The control signal u_2 of the super twisting algorithm is written as follows:

$$u_2 = u_d + u_{eq} \quad (22)$$

Note that u_{eq} is the equivalent control proposed by Vadim Utkin in [24]. It is written as follows:

$$u_{eq} = 1 - \frac{V_{in2}}{V_{out2}} \quad (23)$$

With $V_{in2} = V_{out1}$,

The switching control u_d is the discontinuous function given by equation (24); it is composed of a discontinuous part v_1 given in equation (25) and a continuous part v_2 given in equation (26)

$$u_d = v_1 + v_2 \quad (24)$$

$$v_1 = -\lambda .. |s|^{0.5} .sign(s) \quad (25)$$

$$v_2 = -\gamma .sign(s) \quad (26)$$

With S being the sliding surface (difference between the filtered inductor current and the reference current) given in equation (27)

$$s = i_{sta} - I_{ref2}, with\,(s = I_{L2} - I_{ref2}) \quad (27)$$

λ and γ are positive parameters; the reference current I_{ref2} is obtained using a conventional PI controller and i_{sta} is the modified inductor current.

V. STABILITY PROOF

In this section, we prove the stability of the super twisting control system designed in the previous section. We do this by using a Lyapunov function approach.

A. Invariance Condition

From equation (22), the invariance condition is expressed as:

$$s = 0 \text{ and } s = 0$$

Now, to delve deeper into the analysis, let us consider the derivative of the sliding surface, which is elegantly presented in equation (28):

$$s = I_{L2} - I_{ref2} \quad (28)$$

$$s = x_3 - I_{ref2} \quad (29)$$

$$s = -\frac{(1-u_2).V_{out2}}{L_2} + \frac{V_{out1}}{L_2} - I_{ref2} \quad (30)$$

The importance of these equations becomes evident as we explore further. We can derive:

$$s = -\frac{(1-(u_{eq}+u_n).V_{out2}}{L_2} + \frac{V_{out1}}{L_2} - I_{ref2} \quad (31)$$

$$s = \frac{V_{out2}}{L_2} u_n + \frac{V_{out1} - V_{out2}}{L_2} - I_{ref2} + \frac{V_{out2}}{L_2} u_{eq} \quad (32)$$

B. Derivative of the Sliding Surface

For $s = 0$ and $u_n = 0$, we obtain

$$u_{eq} = 1 - \frac{V_{out1}}{V_{out2}} + I_{ref2} \frac{L_2}{V_{out2}} \quad (33)$$

$$s = \frac{V_{out2}}{L_2} u_n \quad (34)$$

C. Lyapunov Function

Let us choose the Lyapunov function, such as

$$V = \frac{1}{2} s^2 \quad (35)$$

To gauge the stability of this function, we meticulously evaluate its derivative:

$$V = s\,s \quad (36)$$

One must verify the decrease of the Lyapunov function to zero. For this purpose, ensuring that its derivative is negative definite is sufficient.

$$V = s\,s < 0 \tag{37}$$

$$V = \frac{V_{out2}}{L_2} u_n s < 0 \tag{38}$$

Replacing u_n in equation (38)

$$V = \frac{V_{out2}}{L_2} s.(v_1 + v_2) < 0 \tag{39}$$

$$V = \frac{V_{out2}}{L_2} s.(-\lambda.|s|^{0.5}.sign(s) + \int -\gamma.sign(s)dt) < 0 \tag{40}$$

$$V = \frac{V_{out2}}{L_2} .(-\lambda.|s|^{0.5}|s| + \int -\gamma s.sign(s)dt) < 0 \tag{41}$$

Upon careful examination, we confirm:

$$r_{L1} = r_{L2}(\Omega) \tag{42}$$

And V is a negatively definite function. Therefore, the stability is well demonstrated.

VI. EXPERIMENTAL RESULTS

An experimental prototype shown in Fig. 6 is established in the LGEP laboratory to validate the proposed technique. This work uses two boost converters powered by a DC voltage source. IGBT SKM50 GB123D power switches are used. Table I lists the nominal converter's parameters. The control algorithms are digitally implemented in a digital platform (dSPACE1104) that generates the control signals for the switches obtained by the cascaded PI and super-twisting controllers. Table II shows the control parameters of the two cascaded converters.

The experimental prototype (Fig. 6) consists of the following items:

- dSPACE 1104
- An autotransformer as the main grid
- Inductors
- Capacitors
- Variable resistor
- Semikron based on IGBT SKM50 GB123D
- Driver's DC supply
- Adapter card
- Electronic card to sense the currents (LEM LA55-P) and voltages (LEM LV25-P).

Three tests were conducted to assess the efficiency of the proposed technique. The first test involved applying the suggested method to two power levels by injecting the fundamental and a gain G equal to 2. The second test examined the effect of a variation of the gain G multiplied by the fundamental on the voltages and currents of the two cascaded choppers. The last test involved checking the impact of a load resistance variation on the proposed technique while keeping the gain G and input voltage fixed. In these tests, we tried to use a frequency less than or equal to 10 kHz, because the elevation of the switching frequency induces a significant loss of energy.

A. Application of the Proposed Technique for Two Different Input Voltage

A test was conducted with and without the proposed approach to ensure a fair comparison between the novel and conventional techniques. The test was achieved using a single harmonic injection, precisely the fundamental, and a gain of 2. The test was performed at two distinct input voltage values. Initially, the input voltage of 12 V was amplified to 24 V by the feeder converter. Subsequently, the load converter further boosted this 24 V to 50 V. Secondly, the feeder converter increased the input voltage from 24 V to 45 V. Later, the load converter further elevated the voltage to 90 V.

After each method switch, we examine the evolution of the outputs of the two converters: V_{out1}, V_{out2}, $I_{L2}(I_{out1})$, and I_{out2}.

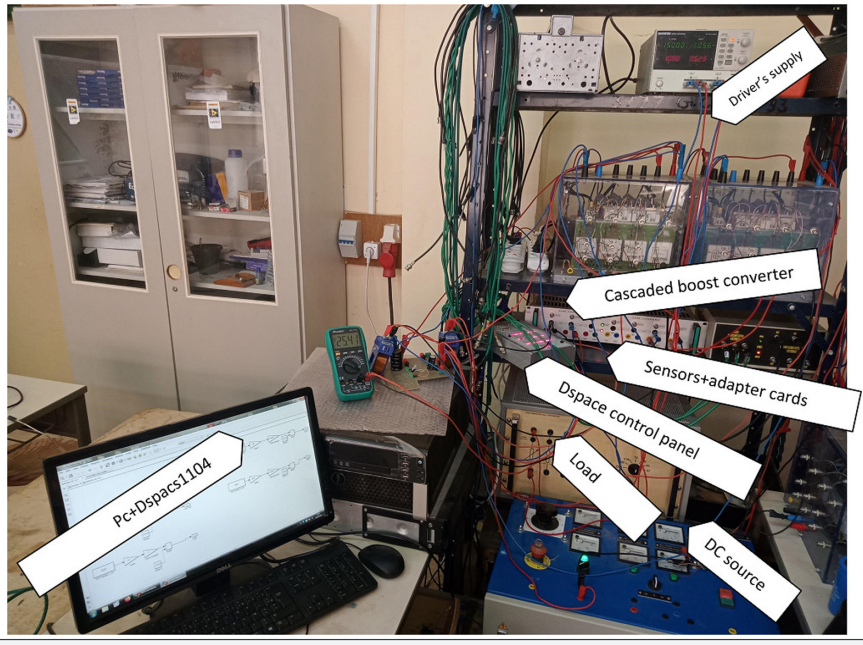

Fig. 6. The experiment prototype.

TABLE I. NOMINAL CONVERTER PARAMETERS

Circuit Parameters	Value
Input voltage, V_{in} (V)	12 and 24
Inductors, $L = L_1 = L_2$ (mH)	1
Internal resistance of inductances $r_L = r_{L1} = r_{L2}(\Omega)$	0.4
Capacitors, $C = C_1 = C_2$ (μF)	470
Load resistor, R_2 (Ω)	55, 73, and 110
The feeder chopper's switching frequency, f_{d1} (KHz)	10
The load chopper's switching frequency, fd_2 (KHz)	5

TABLE II. THE CONTROL PARAMETERS

Cascaded PI Controller	Cascaded PI-Super Twisting Controller
$K_{pv} = 20$	$K_{pv} = 0.8$
$K_{pv} = 0.08$	$K_{pv} = 10$
$K_{pi} = 20$	$\lambda = 1$
$K_{ii} = 0.08$	$\Delta = 0$

Fig. 7 shows the outputs of the first converter (feeder converter). Using a gain of 2, the new super-twisting sliding mode control (STSMC) affected the first converter and reduced the output voltage by 60% and the output current by 73% in the case of $V_{in1} = 12$ V. For $V_{in2} = 4$ V, V_{out1} ripples were decreased by 57%, and I_{out1} ripples by 84% (The ripples ΔV and ΔI are reduced from 10V to 4V and from 5.46 A to 1.5 A in the case of $V_{in1} = 12$ V. In the case of $V_{in1} = 24$ V, the ripples ΔV and ΔI are reduced from 14 V to 6 V and 10 A to 1.65 A).

Fig. 8 shows the outputs of the load converter. The new STSMC reduced this converter's output voltage and current by 48% (ΔV is reduced from 6.08 V to 3.36 V) and by 56% (ΔI is reduced from 0.09 A to 0.05 A) in the case of $V_{in1} = 12$ V. In the case of $V_{in1} = 24$ V, the output voltage and current are reduced by 60% (ΔV is reduced from 10.71 V to 3.83 V) and by 68% (ΔI is reduced from 0.17 A to 0.06 A).

B. Effect of The Gain Variation on The Voltages and Currents of the Two Converters

After confirming the effectiveness of the new STSMC in reducing the ripples of the different voltages and currents in our system, it is time to check the effect of the gain G.

Rising the gain from 1 to 2 had a noticeable effect on the input current of the load converter (the ripple ΔI is reduced from 3.38 A to 1.5 A), and the amount of ripple reduction is about 56%. Other outputs were slightly affected, as shown in Fig. 9.

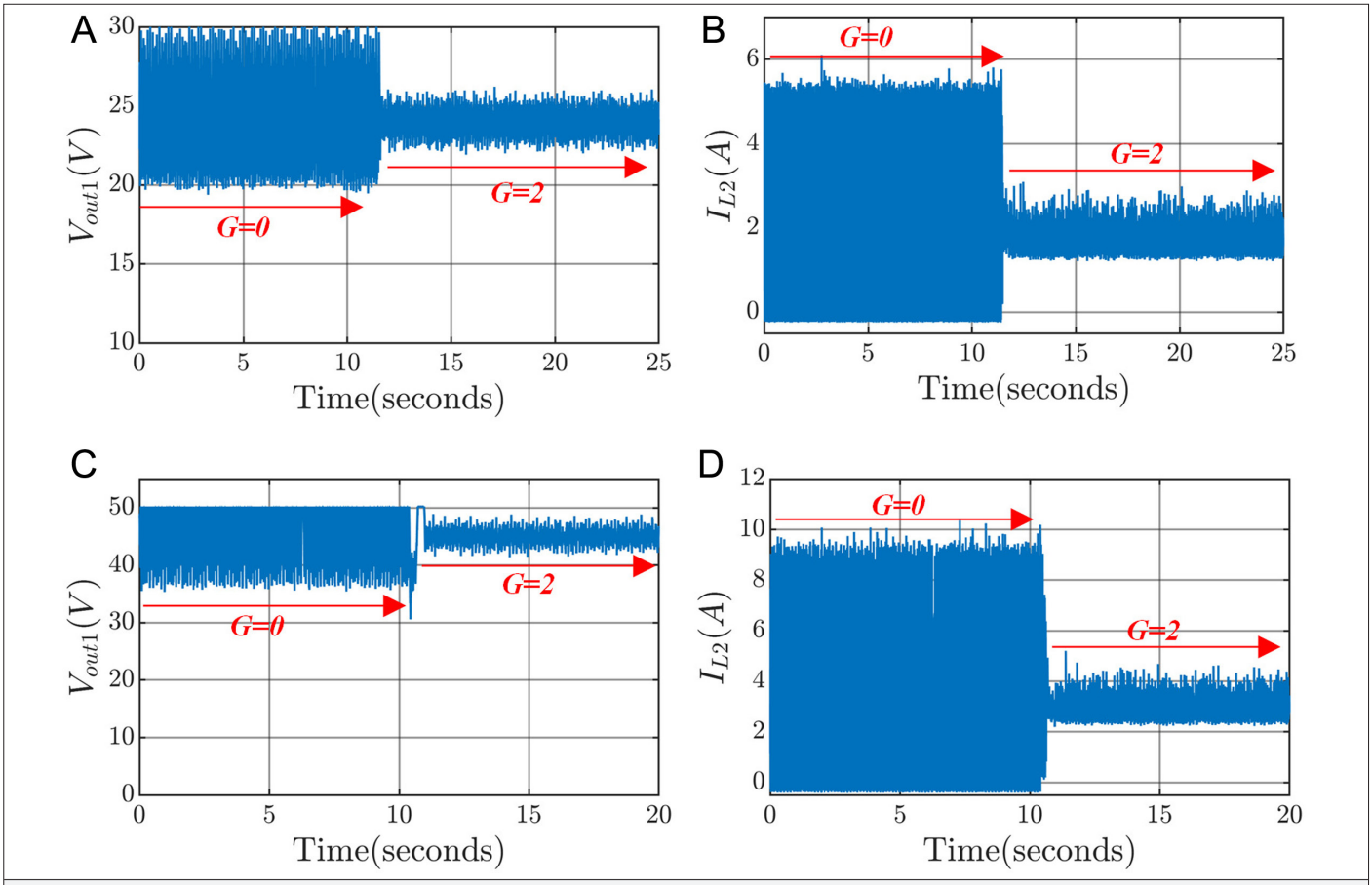

Fig. 7. Outputs of the feeder converter using the conventional STSMC then the new STSMC: $V_{in1} = 12$ V input: (a) The output voltage. (b) The output current. $V_{in1} = 24$ V. (c) The output voltage, (d) The output current.

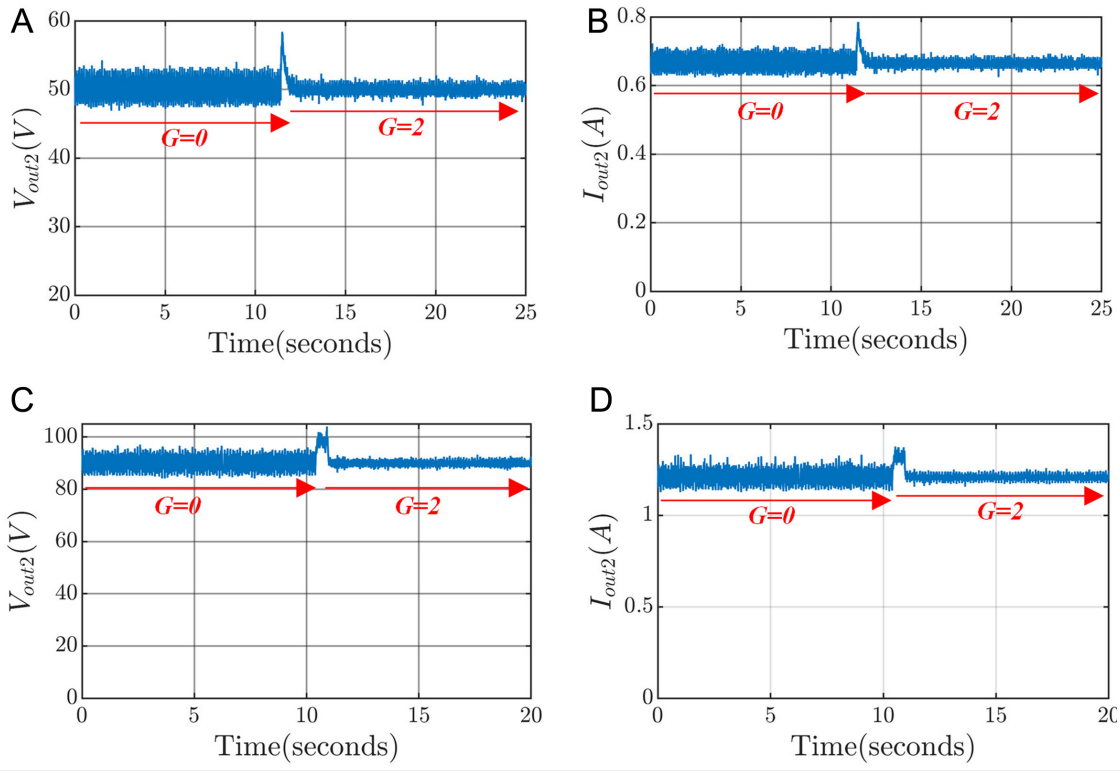

Fig. 8. Outputs of the load converter using the conventional STSMC then the new STSMC: V_{in1} = 12V. (a) The output voltage. (b) The output current. V_{in1} = 24V (c) The output voltage. (d) The output current.

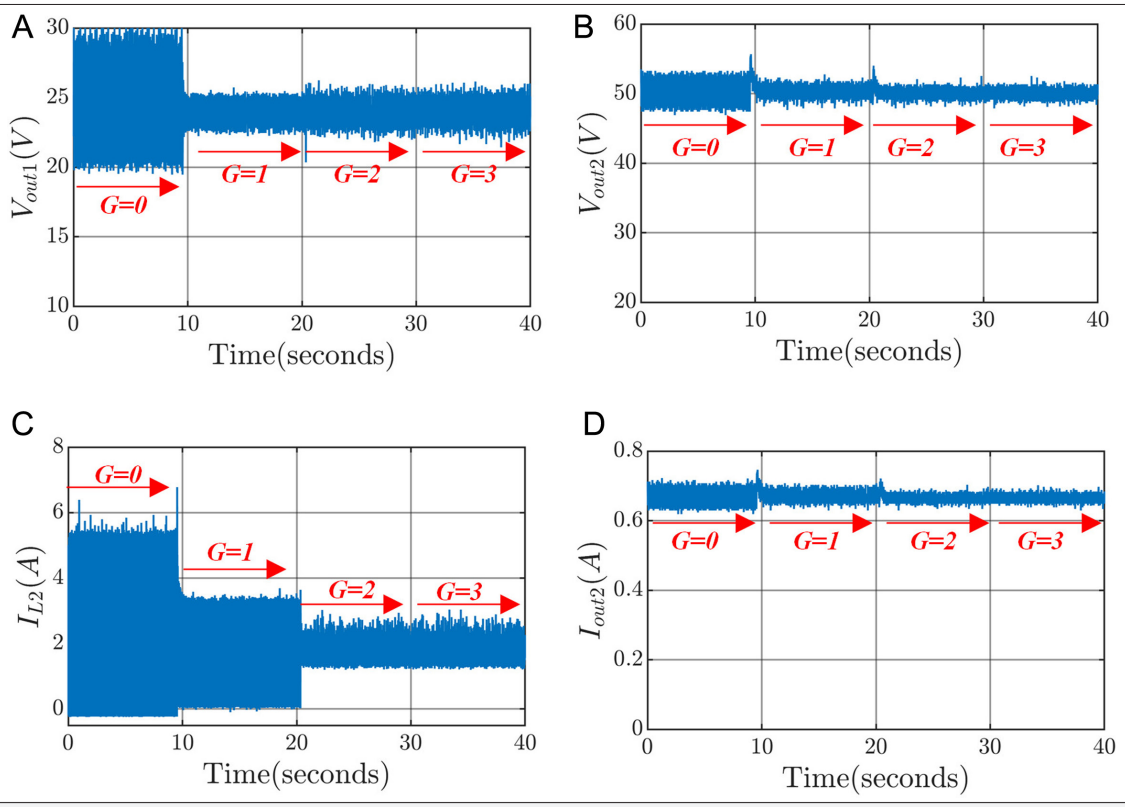

Fig. 9. The effect of increasing the gain G (values 1, 2, and 3). (a) The feeder converter's output voltage. (b) the load converter's output voltage. (c) The load converter's input current. (d) The load converter's output current.

Increasing the gain to 3 did not affect the outputs of the two converters.

C. Control of the Converters Under Load Variation

A robustness test is done in this sub-section, where a load change is applied to our new STSMC. The input voltage for the feeder converter is 12 V, its output is 24 V, and the output of the load converter is 50 V. The gain is fixed at 2.

First, we apply the conventional STSMC. The new STSMC is then applied on a load of 73 Ω afterward, and the load is reduced to 55 Ω, leading to an increase in current. The results of the input and output voltages and currents of the load converter are shown in Fig. 10.

Despite the load change, the current ripple ΔI slightly increased (1.5 A to 1.62 A) but remained largely under the original ripple of 5.46 A.

D. Comparison Assessment With Other Solutions

To calculate the overall circuit efficiency, we need to calculate the power output by the second boost converter and the power absorbed by the first converter, and then we divide it up.

The power output by the second boost converter is equal to 50 V × 0.65 A = 32.5 W. The power absorbed by the first boost converter is equal to 12 V × 3 A = 36 W. So the efficiency is equal to 90.28% (mentioned in the table).

Efficiency without using technique is about 88.09%, and after using the proposed technique it was 90.28%. For the prototype used in this paper, the proposed technique increased the efficiency by 2%.

Efficiency can never reach 100% because in every converter, there are components that reduce efficiency, such as semiconductors (2 diodes and 2 IGBTs (Insulated Gate Bipolar Transistor) in our case). Energy conversion electronics are based on the use of semiconductor components acting as switches. When these switches are in use, they suffer thermal losses corresponding to the various phases of their operation. There are three types of loss, each corresponding to a different state of the switch:

- Conduction losses, associated with the conducting state of the component
- Leakage losses associated with the blocked state of the switch
- Dynamic losses or switching losses are associated with changes in the state of the switch, i.e., when passing from the on state to the off state and vice versa.

These losses cause a considerable reduction in the system's overall performance.

It is interesting to compare some of the solutions done in the past with the work we have done to enhance the value of paper. Table III summarizes the performances of the ripple minimization technique mentioned in the literature, control method, efficiency

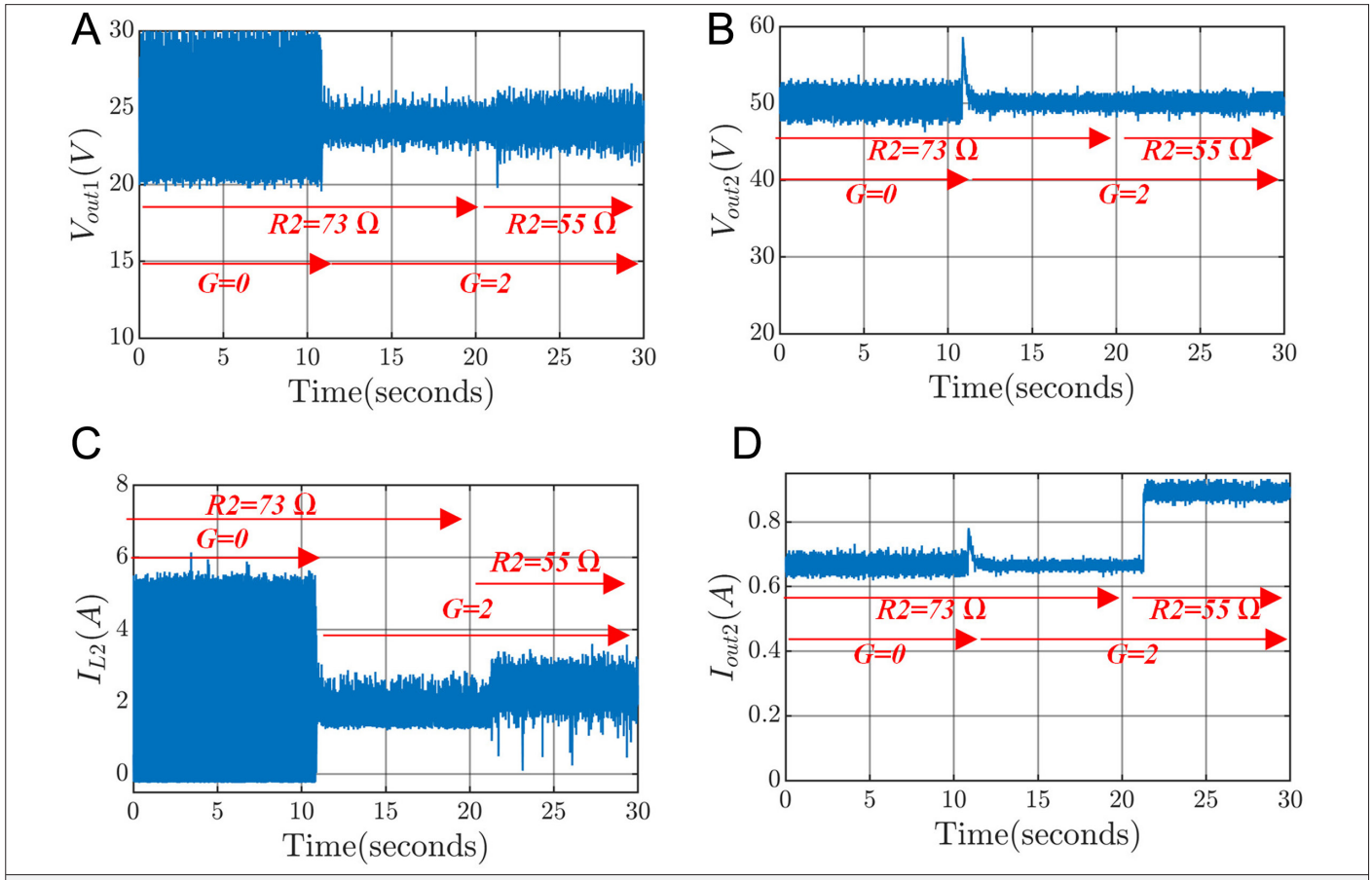

Fig. 10. Load change test with a gain G = 2. (a) The feeder converter's output voltage. (b) the load converter's output voltage. (c) The load converter's input current. (d) The load converter's output current.

TABLE III. COMPARISON OF THE PROPOSED CONTROLLER'S PARAMETERS WITH VARIOUS CONTROLLERS USED IN THE HIGH GAIN BOOST CONVERTER

References	Topology	Active/Passive Damping or New Converter Topology	Control	Voltage Gain	Amount of Ripple Reduction	L/C	S/D	Total	Efficiency (%)
[12]	Two-stage cascaded boost converter	Active	A classic controller PI	4	Inductor current not measured	2/2	2/2	8	Not mentioned
[17]	Two-stage cascaded boost converter	Active	Flatness Based Decentralized Adaptive Backstepping Controller	2	++ for DABC+LPs (Vref variation). + for DABC+LPs (Load variation). ++ for DABC+LPs (E variation). + for SMBC (Vref variation).	2/2	2/2	8	Not mentioned
[25]	Two-stage cascaded boost converter	Active	A feedback controller composed of a comparator and an RS flip-flop	3.5	+++ for SF. ++ for DF.	2/2	2/2	8	Not mentioned
[26]	Two-stage cascaded boost converter	Active	A PI and sliding mode controllers	2	+++	2/2	2/2	8	Not mentioned
[27]	Two parallel boost converters	Passive	A passive feed forward controller is added to the conventional double loop controller	2	+++	2/2	2/2	8	Not mentioned
[28]	A new dual-input high step-up DC–DC converter	New converter topology	A classic controller PI	14.64	+++	2/5	2/4	13	96.35
[29]	An ultra-high gain DC/DC boost converter with a modified voltage multiplier cell (VMC)	Active	A classic controller PI	9.75	+++	2/6	1/7	16	95.4
[30]	CI-SIDO boost converter	Active	The controller is implemented in FPGA mainly using registers, discrete counters and comparators	2.25	+++	2/2	2/2	8	87.5
[31]	A new single-switch non-isolated DC/DC converter	New converter topology	A conventional PWM technique at a constant frequency	10	+++	2/4	1/3	10	95.8
Proposed	Two-stage cascaded boost converter	Active	A PI and a new super twisting controllers.	4	++ for G = 1. +++ for G = 2. +++ for G = 3.	2/2	2/2	8	90.28

measurement, and voltage gain ratio. Metrics displayed in Table III are taken from data provided by authors in their papers.

In [12, 17, 25, 26] and the present paper, the use of two classic boost converters operating in cascade increased the voltage gain between 2 and 4, using the same number of diodes, switches, inductors, and capacitors. Since the inductor current in Ref. 12 is not measured, its ripple could not be determined. In [17], for a variation of input or output voltage, the DABC + LPs allow a slight reduction of the current ripple, while the SMBC does not give a good reduction. In [25], the current ripples are reduced for different frequencies and are well reduced for the same frequencies, but the control method is a bit more complex. Although the current ripples are well reduced in [26], using high frequencies (100 KHz) can increase the energy losses, reducing the system's efficiency. The passive controller is added to the traditional double loop regulator in [27] to control the two converters that are connected in parallel. Power dissipation is the issue with this kind of control, even though it permits very little current ripple. The use of a new topology, a new dual-input high-amplification-rate DC–DC converter controlled by a conventional pi regulator with an efficiency of 96.35% [28] and an ultra-high-gain DC/DC boost converter with a modified voltage-multiplying cell with an efficiency of 95.4% [29], provides high voltage gain with reduced current ripple. However, the drawback of these two works is the use of a large number of components. The CI-SIDO (Coupled Inductor Signle Input Dual Output) converter presented in [30] allows a voltage gain of 2.25 with a reduced number of components (8) and a low current ripple with an efficiency of 87.5%. The new non-isolated single-switch DC/DC converter used in [31] allows for a high voltage gain with low current ripple while using 10 components with an efficiency of 95.8%. In this work, the two-stage cascaded boost converter structure is employed with several

forms of control. In this case, the voltage gain is equal to 4 with an efficiency of 90.28%, and the current ripple is well reduced after using the new inductor current ripple minimization technique. Compared to the state-of-the-art ripple minimization techniques, our method employs the converter's measured variable without the need for additional hardware or complex mathematical procedures. Moreover, it is robust to input and output voltage changes.. In addition, the quality improvement effect of the current and/or voltage comes from both the load converter side and the power converter side.

E. Discussion

Experimental tests shown above gave insight into the merits of the new STSMC. Our main goal was to reduce the input current of the load converter (IL2 or I_{out1}). However, lowering the input voltage (V_{out1}) and hence the output current and voltage (I_{out2} and V_{out2}) was a by-product of this operation.

Fig. 11 visually presents the experimental test results. To represent the amount of ripple reduction, a new quantity has been bar plotted; this quantity is defined as:

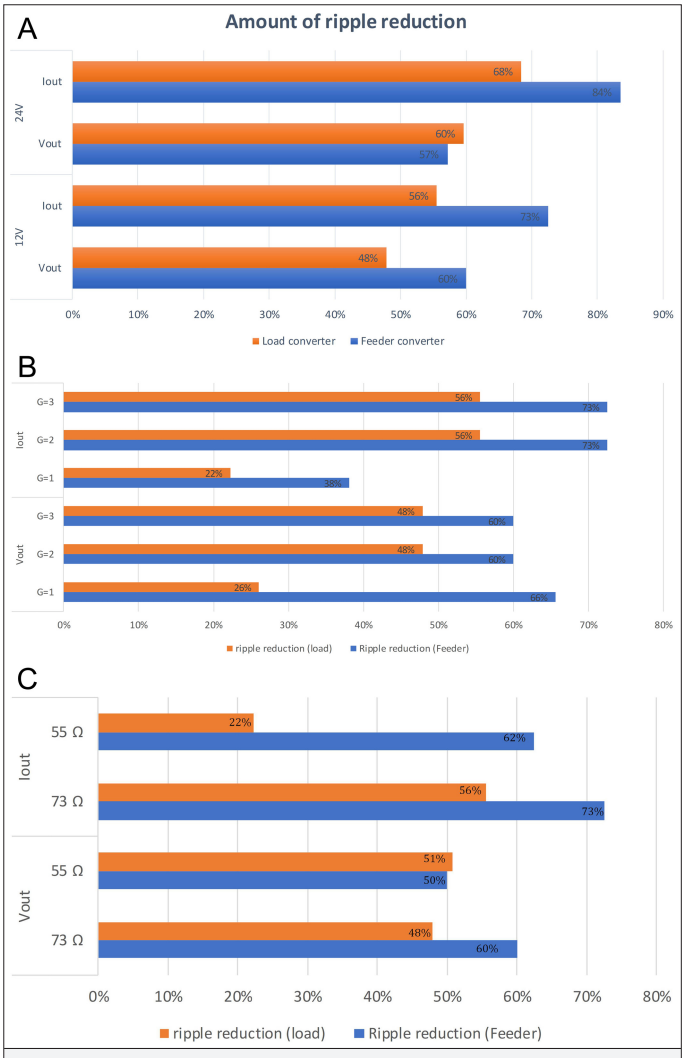

Fig. 11. Ripple reduction in the case of (a) voltage change, (b) gain change, (c) load change.

$$\text{Amount of ripple reduction} = \frac{\Delta X_{STSMC} - \Delta X_{new-STSMC}}{\Delta X_{STSMC}} \quad (43)$$

Analyzing the experimental results yields the following conclusions:

- The modified super twisting is robust to input and output voltage changes.
- The input voltage of the load converter has been increased from 24 V to 45 V resulting in a change of the output voltage from 50 V to 90 V. Even though there was a surge in ΔI, the proposed modified super twisting kept a high current ripple reduction.
- As mentioned at the beginning of the section, reducing the input current affected the other currents and voltages, resulting in a positive ripple reduction in these outputs.
- A gain of 2 is the optimal gain. We noticed a surge in ripple reduction (Fig. 11(b)) when we increased the gain from 1 to 2. Further increases had no effect.
- The modified super twisting moved the load converter's inductor current away from 0, making it a suitable method to avoid discontinuous conducting mode.

VII. CONCLUSION

This paper presents a new method for reducing ripples in a cascaded DC/DC converter. The focus is reducing the second stage's input ripple in a cascaded DC/DC boost. To achieve this, a modified STSMC is used, which feeds back a weighted fundamental component of the second-stage input current to reduce the input current. This reduces ripples in both the input and output voltage and current of the second stage. The novelty of this technique is the choice of the sliding surface. The technique is part of active damping approaches, does not require additional sensors or passive components, and reduces system cost. The method improves the load and power converter sides' current and/or voltage quality. It is easy to implement and is applicable to various loads and power levels. Additionally, it provides a voltage gain of 4 for frequencies of 10 kHz or less and is robust to input and output voltage changes. Experimental tests have confirmed its effectiveness, with a gain of 2 being the optimal result.

Peer-review: Externally peer-reviewed.

Author Contributions: Concept – K.K., A.S.; Design – K.K., A.G.; Supervision – A.S., A.G., Y.M.; Data Collection and/or Processing – A.C.; Analysis and/or Interpretation – K.K., A.S., A.G., D.O.; Writing – K.K.; Critical Review – A.S., A.G., Y.M., D.O., A.C.

Declaration of Interests: The authors have no conflict of interest to declare.

Funding: The authors declare that this study received no financial support.

REFERENCES

1. T. Dragicevic, X. Lu, J. Vasquez, and J. Guerrero, "DC microgrids— Part I: A review of control strategies and stabilization techniques," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4876–4891, 2016. [CrossRef]
2. H. Nikkhajoei, and R. H. Lasseter, "Distributed generation interface to the CERTS microgrid," *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 1598–1608, 2009. [CrossRef]
3. R. H. Lasseter, "Microgrids and distributed generation," *Intell. Autom. Soft Comput.*, vol. 16, no. 2, pp. 225–234, 2010. [CrossRef]
4. S. Ali, Z. Zheng, M. Aillerie, J. P. Sawicki, M. C. Péra, and D. Hissel, "A review of DC microgrid energy management systems dedicated to residential applications," *Energies*, vol. 14, no. 14, pp. 4308, 2021. [CrossRef]
5. D. Kumar, F. Zare, and A. Ghosh, "DC microgrid technology: system architectures, AC grid interfaces, grounding schemes, power quality,

communication networks, applications, and standardizations aspects," *IEEE Access*, vol. 5, pp. 12230–12256, 2017. [CrossRef]
6. Y. Han, X. Ning, P.Yang, and L. Xu, "Review of power sharing, voltage restoration and stabilization techniques in hierarchical controlled DC microgrids," *IEEE Access*, vol. 7, pp. 149202–149223, 2019. [CrossRef]
7. A. Kwasinski, and C. N. Onwuchekwa, "Dynamic behavior and stabilization of DC microgrids with instantaneous constant power loads," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 822–834, 2011. [CrossRef]
8. Q. Xu, C. Zhang, C. Wen, and P. Wang, "A novel composite nonlinear controller for stabilization of constant power load in DC microgrid," *IEEE Trans. Smart Grid*, vol. 10, no. 1, pp. 752–761, 2017. [CrossRef]
9. S. Singh, A. R. Gautam, and D. Fulwani, "Constant power loads and their effects in DC distributed power systems: a review," *Renew. Sustain. Energy Rev.*, vol. 72, pp. 407–421, 2017. [CrossRef]
10. Q. Xu, N. Vafamand, L. Chen, T. Dragičević, L. Xie, and F. Blaabjerg, "Review on advanced control technologies for bidirectional DC/DC converters in DC Microgrids," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 2, pp. 1205–1221, 2020.
11. E. Hossain, R. Perez, A. Nasiri, and S. Padmanaban, "A comprehensive review on constant power loads compensation techniques," *IEEE Access*, vol. 6, pp. 33285–33305, 2018. [CrossRef]
12. H. Li *et al.*, "A describing function-based stability analysis method for cascaded DC-DC converters," *IEEE Open J. Ind. Electron. Soc.*, vol. 3, pp. 484–495, 2022. [CrossRef]
13. S. Luo, "A review of distributed power systems part I: DC distributed power system." *IEEE Aerosp. Electron. Syst. Mag.*, vol. 20, no. 8, pp. 5–16, 2005. [CrossRef]
14. A. El Aroudi, D. Giaouris, H. Ho-Chinglu, and I. A. Hiskens, "A review on stability analysis methods for switching mode power converters", *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 5, no. 3, pp. 302–315, 2015.
15. R. Xu, Y. Zhang, L. Wang, G. Chen, S. Liu, and H. Wen, "Research on slow-scale bifurcation phenomenon of PFC cascade converter," *IET Power Electron.*, vol. 9, no. 15, pp. 2824–2832, 2016. [CrossRef]
16. S. Dutta, and B. Johnson, "A practical digital implementation of completely decentralized ripple minimization in parallel-connected DC–DC converters," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14422–14433, 2022. [CrossRef]
17. S. Shoja, "Flatness-based decentralized adaptive backstepping control of cascaded DC–DC boost converters using Legendre polynomials", *J. Control Autom. Electr. Syst.*, vol. 31, no. 6, pp. 1533–1548, 2020.
18. K. Miao, Y. Zhang, J. Zhang, S. Fan, and X. Yin, "Virtual RC feedforward control strategy for constant power load in marine DC microgrid," in Power System and Green Energy Conference (PSGEC), Vol. 2022, 2022, pp. 565–570. [CrossRef]
19. R. Stala, Z. Waradzyn, and S. Folmer, "Input current ripple reduction in a step-up DC–DC switched-capacitor switched-inductor converter," *IEEE Access*, vol. 10, pp. 19890–19904, 2022. [CrossRef]
20. D. Ertekin, "A high gain switched-inductor-capacitor DC-DC boost converter for photovoltaic-based micro-grid applications," *CSEE J. Power Energy Syst.*, pp. 1-10, 2023. [CrossRef]
21. H. Sira-Ramirez, and R. Silva-Origoza, *Control Design Techniques in Power Electronics Devices*. Springer, 2006.
22. W. E.Robert, and M. Dragan, *Fundamentals of Power Electronics*. Kluwer Academic Publishers, 2001.
23. S. Zhuo, A. Gaillard, Q. Li, R. Ma, D. Paire, and F. Gao, "Current ripple optimization of four-phase floating interleaved DC–DC boost converter under switch fault," *IEEE Trans. Ind. Appl.*, vol. 56, no. 4, pp. 4214–4224, 2020. [CrossRef]
24. V. I. Utkin, "Sliding mode control of DC/DC converters," *J. Franklin Inst.*, vol. 350, no. 8, pp. 2146–2165, 2013. [CrossRef]
25. H. Ji, F. Xie, Y. Chen, and B. Zhang, "Small-step discretization method for modeling and stability analysis of cascaded DC–DC converters with considering different switching frequencies," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 8855–8872, 2022. [CrossRef]
26. Z. Chen, W. Yong, and W. Gao, "PI and sliding mode control of a multi -input-multi-output boost-boost converter," *WSEAS Trans. Power Syst.*, vol. 9, pp. 87–102, 2014.
27. F. Li, and Z. Lin, "Novel passive controller design for enhancing boost converter stability in DC microgrid applications," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 6, pp. 6901–6911, 2021. [CrossRef]
28. A. Samadian, S. M. Hashemzadeh, M. G. Marangalu, M. Maalandish, and S. H. Hosseini, "A new dual-input high step-up DC–DC converter with reduced switches stress and low input current ripple," *IET Power Electron.*, vol. 14, no. 9, pp. 1669–1683, 2021. [CrossRef]
29. S. Khan *et al.*, "A new transformerless ultra high gain DC–DC converter for DC microgrid application," *IEEE Access*, vol. 9, pp. 124560–124582, 2021. [CrossRef]
30. N. Nupur, and S. Nath, "Minimizing ripples of inductor currents in coupled SIDO boost converter by shift of gate pulses, *IEEE Trans. Power Electron.*, Vol. 35, no. 2, 2019, pp. 1217–1226.
31. M. A. Al-Saffar, and E. H. Ismai, "A high voltage ratio and low stress DC–DC converter with reduced input current ripple for fuel cell source," *Renew. Energy*, vol. 82, pp. 35–43, 2015. [CrossRef]

Khadidja Khattab was born in Tiaret, Algeria, on April 15, 1995. She obtained a master's degree in electrical engineering from the Université Ibn Khaldoun in Tiaret in 2019 and is currently pursuing her doctorate at the Université Ibn Khaldoun in Tiaret, Algeria. Her work focuses on DC microgrids, DC–DC converter control, and power quality improvement.

Ahmed Safa received his engineering degree and MSc (diploma) degree in electrical engineering from University Ibn Khaledoun Tiaret, Algeria, in 2009 and 2012, respectively, and the PhD degree from the Ecole Nationale Polytechnique of Algiers, in 2017. He is currently teaching with the Ibn Khaldoun University of Tiaret and conducting his research at LGEP, Tiaret. His power quality and synchronization, especially when employed for renewable energy systems.

Abdelmadjid Gouichiche received his engineering and MSc degrees in electrical engineering from the Ibn Khaldoun University of Tiaret, Algeria, in 2007 and 2010, respectively, and the Ph.D. degree from the National High Polytechnic School of Algiers, in 2015. He is currently an assistant teacher with the Ibn Khaldoun University of Tiaret and the head of the Research Laboratory LGEP. His research interests include fault-tolerant control of electrical machines and DC/DC converters.

Youcef Messlem was born in Tiaret in 1969. He received his engineering degree in electrotechnics from Ibn Khaldoun University, in 1992, and his DEA degree and the Doctorat d'Etat (PhD) degree in electrical engineering from Paris VI University, France, in 1994 and 1998, respectively. He joined the Electrical Engineering Department, Ibn Khaldoun University, in 1999. His research interests include electrical drives, high voltage, and power systems. Dr. Messlem is a member of the Laboratory Genie Electrique et des plasmas (LGEP).

Djaffar Ould Abdeslam (M'08–SM'15) was born in Tizi-Ouzou, Algeria, on April 20, 1976. He received his MSc degree in electrical engineering from the University of Franche-Comté, Besançon, France, in 2002. He received the PhD degree in 2005 and the Habilitation degree in electrical engineering in 2014 from the University of HauteAlsace, Mulhouse, France. Since 2007, he has been an associate professor at the University of Haute-Alsace. His research interest includes artificial neural networks applied to power systems, signal processing for power quality improvement, smart metering, smart building, and smart grids.

Abdelilah Chibani received his master's and bachelor's degree in electrical engineering from the Ibn Khaldoun University of Tiaret, Algeria, in 2011 and 2013, respectively, and the PhD degree from the Ibn Khaldoun University of Tiaret, Algeria, in 2018. He is also a member of the LGEP Laboratory, Tiaret. His research interests include the control and observation of chaotic system and fault-tolerant control of electrical machines.