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Grounded Meminductor Emulator using a Single Active Building Block and Its Application

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ABSTRACT

This paper presents a grounded meminductor emulator that integrates a dual-X current conveyor differential input transconductance amplifier (DXCCDITA), a grounded memristor emulator, and a capacitor. Utilizing a single DXCCDITA unit eliminates the requirement for multiple building blocks and allows the exploitation of its inherent electronic tunability. The circuit's performance was verified through a comprehensive evaluation across a wide frequency range. The simulations were conducted using the LTspice tool and a 0.18 µm complementary metal-oxide-semiconductor technology platform. Furthermore, the proposed meminductor emulator is employed to develop a chaotic oscillator. The satisfactory outcomes obtained from evaluating the meminductor emulator in all aspects of the circuitry, as well as its practical application, validate its suitability in real-world scenarios.

***Index Terms*—**Dual-X current conveyor differential input transconductance amplifier (DXCCDITA), meminductor, memristor emulator, chaotic oscillator

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I. INTRODUCTION

The discovery of memristors by Professor L. Chua in 1971, leading to their first physical implementation with TiO2 in 2008 by HP Labs, has broadened the discourse surrounding the fourth fundamental circuit element [1]. The introduction of the fourth fundamental circuit element, namely the memristor, has bridged the technological gap among hardware components. Limitations observed in power-intensive computer applications have prompted discussions on traditional digital computing architectures [2]. The restrictions of CMOS circuits [3], along with physical distances between memory chips and processing units, have resulted in increased power consumption and latency. A comparative analysis of CMOS and TTL technology demonstrates significant advancements in performance and the size of electronic devices [4]. However, concerns such as switching speeds, increased parasitic effects, and sizing limitations in CMOS have compelled researchers to explore alternatives. The proposition is made for the utilization of nanoscale analog devices, such as memristors and broader memelements, as a means to overcome the limitations mentioned above [5]. These devices bring forth novel computing paradigms founded upon in-memory and analog computation principles. By virtue of their non-volatility and non-linearity characteristics, they enable the retention of data in memory without the need for a continuous power supply, while also facilitating the generation of oscillatory and intricate dynamics. These characteristics are particularly valuable for applications such as random number generation, neural chips, and the development of neuromorphic circuits. Professor L. Chua has already proposed circuits demonstrating how memelements can contribute to achieving sub-nanometer sizing and hybrid circuits without the need to shrink the transistors. Breaking away from traditional methods delineated in references [6-18], our circuit architecture adeptly navigates complexity by leveraging a single dual-X current conveyor differential input transconductance amplifier (DXCCDITA), eliminating the necessity for multiple building blocks. The proposed meminductor block follows suit, depending solely on a combination of single active and passive elements. Furthermore, our proposed emulator design distinguishes itself from previous iterations documented in reference [19] by forgoing the need of a TiO_2-based circuit in its implementation. The inherent electronic tunability of the proposed circuit sets it apart from the available meminductors

detailed in [20]. The tunability through only two components, namely the I_{bias} and the V_z terminals, supports the flexibility of the proposed meminductor. The seamless operation in both grounded and floating modes, as observed in [21] underscores a versatile functionality—a facet notably absent in emulators chronicled in [22], which predominantly adhere to grounded mode operation. The proposed circuit represents a notable departure from the conventional methods seen in meminductor emulators, which commonly rely on multipliers. Furthermore, it achieves an impressive operating frequency, surpassing the capabilities of many previously suggested circuits. However, it is imperative to acknowledge the inherent limitations of this meminductor emulator, underscoring the need for careful consideration in both its application and ongoing development. Several researchers have proposed various memelement emulators using active building blocks, including operational transconductance amplifiers (OTAs) [23], operational amplifiers (OPAMPs) [24], current feedback operational amplifiers (CFOAs) [25], second-generation current conveyors (CCIIs) [26], differential-difference current conveyors (DDCCs) [27], current conveyor transconductance amplifiers (CCTAs) [28], differential voltage current conveyor transconductance amplifiers (DVCCTAs) [29], voltage difference transconductance amplifiers (VDTAs) [30], voltage differencing inverting buffered amplifiers (VDIBAs) [31], current follower differential input transconductance amplifiers (CFDITAs) [32], voltage differencing current conveyors (VDCCs) [33], etc. Many emulator-based on active building blocks show high circuit complexity and power consumption. Recent advances in meminductor devices surpass previous studies, revealing characteristics like frequency-dependent hysteresis. Our work combines memristor and meminductor emulators with a capacitor to meet frequency requirements. The use of a memristor emulator enables us to achieve crucial frequencies.

A. Memelements and Their Equivalent Relations

Figure 1 depicts the relationships among the memory-retaining components. Various memory elements, including memristors, meminductors, and memcapacitors, are crucial in digital and analog electronics. This study focused on meminductor devices and their applications. Passive devices, such as resistors, capacitors, and inductors, follow Ohm's law with current and voltage. This principle also applies to non-linear devices such as memristors, meminductors, and memcapacitors [34].

Equations (1) to (7) elucidate the behavior of these elements.

TABLE I. THE ASPECT RATIOS OF MOSFET

Transistor	Width (μm)	Length (μm)
M1-M2	1.4	0.7
M3-M5	2.8	0.7
M14-M15	2.4	0.7
M16-M18	4.8	0.7
M12-M13	9.6	0.7
M19-M20	9.6	0.7
M6-M11	9.6	0.7
M21-M32	2	1

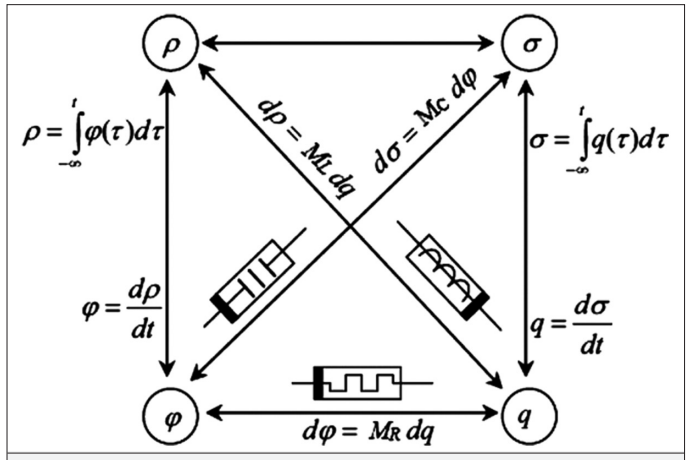

Fig. 1. Correlation among circuit parameters for memory elements.

$$d\varphi = M_R dq \tag{1}$$

$$\varphi = \int_{-\infty}^{t} M_R dq \tag{2}$$

Equation (1) represents the hysteresis relation between flux and charge in a memristor. Upon differentiation with respect to time (t), (1) is equivalent to (3).

$$V(t) = M_R I(t) \tag{3}$$

Where M_R = the memristance of the memristor.

Similarly, a memcapacitor and meminductor element also exhibit the capacity to store and reflect analogous behaviors, as evidenced by the following equations

$$\sigma(t) = \int_{-\infty}^{t} q(t)dt \tag{4}$$

$$\varphi(t) = \int_{-\infty}^{t} q(t)dt \tag{5}$$

Equation (4) represents the hysteresis relation between charge and voltage in a memcapacitor.

$$d\sigma = M_c d\varphi \tag{6}$$

Where M_c represents the memcapacitance of a memcapacitor, which is similar to the Ohm's relation of a capacitor circuit, $q(t) = \int_{-\infty}^{t} i(t)dt$. Which on redefining elucidate as: $q(t) = M_c V(t)$

For a meminductor:

$$d\rho = M_L dq \tag{7}$$

M_L represents the meminductance of the meminductor, analogous to the impedance relationship of a conventional inductor, $\varphi(t) = \int_{V}^{t} v(t)dt$. Which on redefining elucidate as: $\varphi(t) = M_L I(t)$

The above equations represent the behavior of memelements. These memelements are recognized for their robust non-volatile behavior, retaining their state even when power is turned off or

disconnected. The schematic representation in Fig. 1 illustrates the interconnections between these constituent elements. The two novel variables ρ and σ correspond to the temporal integration of flux and charge respectively and are defined by the subsequent relationships.

Memelements, due to their pronounced non-linearity, display intricate dynamics and are suitable for chaotic oscillator circuits [35]. They share similarities with the memristor element, particularly in their benefits for creating artificial synapse circuits. Memelements are also valuable in analog circuits where there's a need to adjust gain and frequency attributes. In the emulation of memelements, two primary methodologies are commonly employed. The first emulator circuit aims to replicate the behavior of memcapacitors and meminductors, utilizing complex arithmetic analog circuitry. However, the intricacy and physical bulkiness associated with such designs have spurred the search for more streamlined alternatives. The second method involves designing an emulator circuit that models the memristor element to replicate the behavior of meminductors or memcapacitors. To reduce the circuit complexity, the second methodology has been adopted. The proposed meminductor emulator circuit emerges as a response to these challenges, offering a solution that is both efficient and effective [36].

II. CHARACTERISTICS OF DUAL-X CURRENT CONVEYOR DIFFERENTIAL INPUT TRANSCONDUCTANCE AMPLIFIER BLOCK

The DXCCDITA was developed to address the limitations of traditional inductors in analog circuits, such as their bulky nature, resistive losses, and limited quality factors when implemented monolithically. The new active element facilitates the design of both grounded and floating inductor simulators, which are essential in modern electronic applications. The DXCCDITA block is characterized by its linearity, ensuring precise signal processing, and its low voltage requirements. With a broad frequency range, this block proves effective across various applications. Its minimal noise levels contribute to a clear signal, crafted for resilient performance. The characteristics of the DXCCDITA block can be precisely defined using the matrix (8).

$$\begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & g_m & 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X+} \\ I_{X-} \\ V_{Z+} \\ V_{Z-} \\ V_O \end{bmatrix} \quad (8)$$

The DXCCDITA block offers designers enhanced flexibility, attributed to the presence of contrasting voltages at the two autonomous X nodes, coupled with inherent adjustability. The differential input structure of *X*+ and X– nodes enables the processing of signals in both non-inverting and inverting modes simultaneously. This characteristic renders the DXCCDITA a versatile component in analog circuit design, especially in applications necessitating differential signal processing. The standalone output terminals, labeled as *Z*+ and *Z*– in Fig. 2, which are linked to OTA inputs, offer the advantage of differential input. The DXCCDITA, which merges the input transconductance amplifier with the OTA, attains exceptional noise performance while reducing all parasitic impacts. In previous works, the DXCCDITA was utilized in designing eight topologies of lossy and lossless grounded inductor simulators and two topologies of floating inductor simulators. The grounded simulators required only two passive elements and a single active block, while the floating simulators required one or three grounded passive elements along with the active block. These designs leverage only grounded capacitors, which is beneficial for fabrication and noise cancellation.

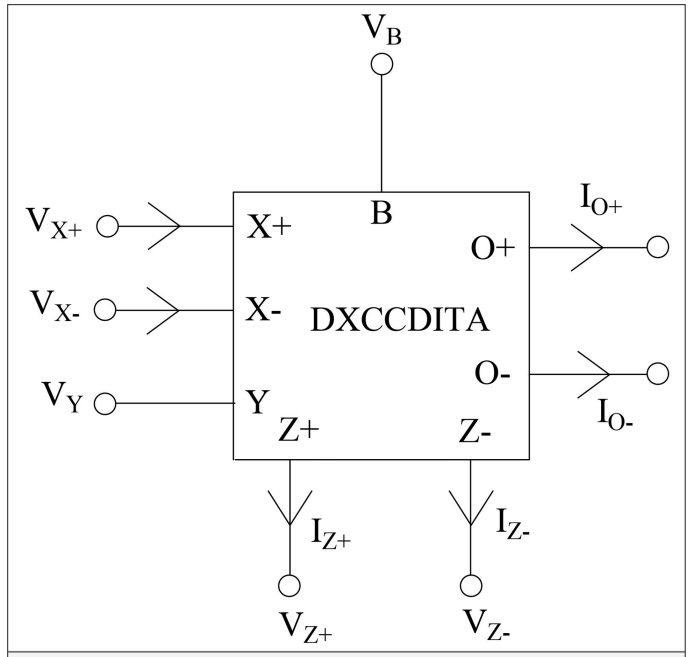

Fig. 2. Dual-X current conveyor differential input transconductance amplifier block [21].

A. CMOS Implementation of Dual-X Current Conveyor Differential Input Transconductance Amplifier Block

The CMOS implementation of the DXCCDITA active block utilized on LTspice 0.18 μm CMOS technology is depicted in Fig. 3. The circuit is bifurcated into two segments; the initial part consists of dual-X second generation current conveyor (DXCCII) [37] which is realized using MOSFETs M1-M20. The voltage at Y can be detected at the V_{X+} pin, while its inverse can be found at the V_{X-} pin.

$$V_{X+} = V_Y \quad (9)$$

$$V_{X-} = -V_Y \quad (10)$$

The current input at the *X*+ node is relayed to nodes *Z*+, and the current from the X– node is directed to Z–.

$$I_{Z+} = I_{X+} \quad (11)$$

$$I_{Z-} = I_{X-} \quad (12)$$

Nodes Y and Z display high impedance, while the X+ and X– nodes show low impedance. The OTA is encompassed within the second section. The transconductance, denoted as g_m is attained through the utilization of MOSFETs M21-M32. The output current of the OTA is contingent upon the voltage disparity between the Z+ and Z– terminals, as dictated by (13).

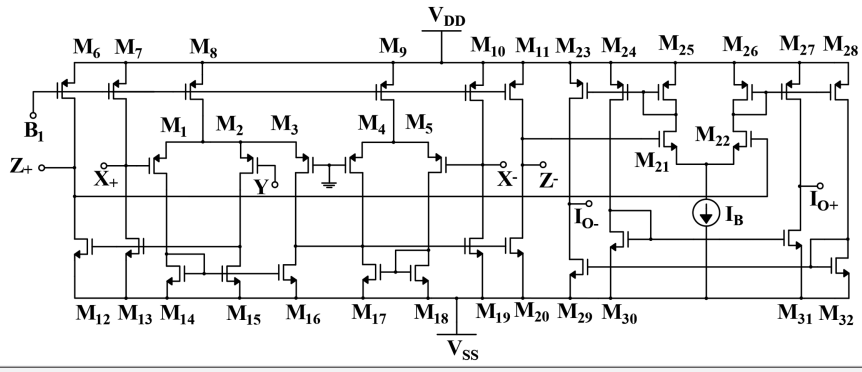

Fig. 3. CMOS-based circuit diagram of dual-X current conveyor differential input transconductance amplifier [21].

III. PROPOSED DUAL-X CURRENT CONVEYOR DIFFERENTIAL INPUT TRANSCONDUCTANCE AMPLIFIER-BASED MEMINDUCTOR IMPLEMENTATION

A novel approach is followed by the proposed meminductor in designing the emulator through the utilization of only three elements: a single active block, one grounded passive element, and a memristor emulator. The resultant current of the proposed meminductor can be determined by employing (13), which is derived from (8).

$$I_{O\mp} = \pm g_m\left(V_{Z+} - V_{Z-}\right) = \pm\left(\sqrt{2I_{Bias}k}\left(V_{Z+} - V_{Z-}\right)\right) \tag{13}$$

Where the transconductance parameter $k = \frac{\mu C_{ox} W}{2L}$, and W is the effective channel width, L is the effective length of the channel, C_{ox} is the gate oxide capacitance per unit area, and μ the carrier mobility. This equation clearly shows the dependency of output current on voltages V_{Z+},V_{Z-} and on the bias current I_{Bias} of the implemented meminductor; that is the adjustment of the meminductor's behavior will only be dependent on these variables. The utilized memristor emulator boasts several advantageous features such as simplicity, easy integration, and the absence of additional external bias requirements. Additionally, the memristor emulator circuit, realized by using the p-channel metal-oxide semiconductor (PMOS)-based diode connected load and RC circuit is utilized in the design of the proposed meminductor emulator. The overall impedance of the utilized memristor emulator, as stated in [38] can be given in (14):

$$M_R(s) = \frac{1}{k\left(v_{c_2} - v_{in} - v_{tp}\right)} + \frac{R}{1 + sRC_2} \tag{14}$$

From the above equation, the impedance is dependent on the voltages across capacitor C_2 and resistor R. The variable resistance provided by the PMOS can be adjusted by modifying the aspect ratios.

In our work, the input has been applied to the Y port of the active block.

$$V_Y = V_{in} \tag{15}$$

The terminals V_{X-}, V_{Z-}, and I_{O+} have been grounded, as illustrated in Fig. 4. On applying Thevenin's theorem, at terminal I_{O-}

$$I_{O-} = I_{in} = \frac{V_{in}}{M_L} \tag{16}$$

Where M_L is the impedance of the proposed meminductor, also for terminal $X+$

$$I_{Z+} = \frac{V_{Z+}}{X_C} \tag{17}$$

Where X_C is the impedance offered by the capacitor at terminal Z+.

For terminal $X+$:

$$I_{X+} = \frac{V_{X+}}{M_R} \tag{18}$$

hence, on comparing (11), (17), and (18).

$$V_{Z+} = \frac{V_{X+}}{M_R}.\left(X_c\right) \tag{19}$$

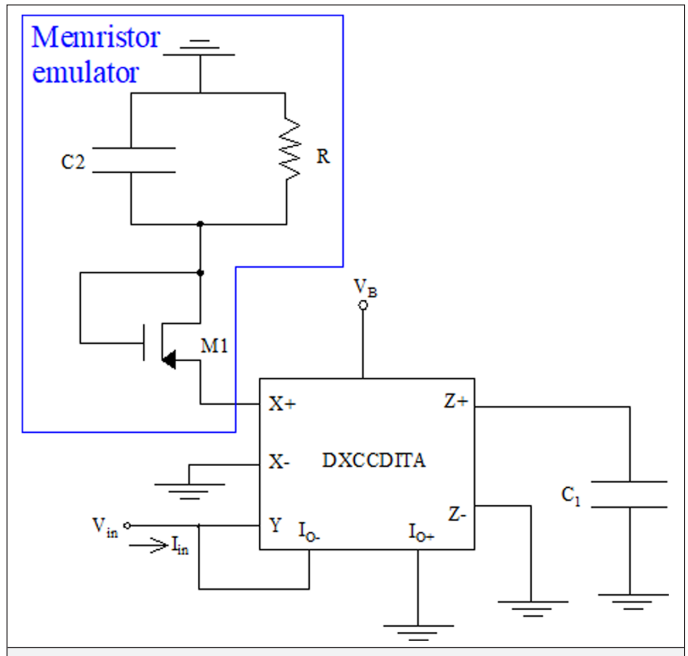

Fig. 4. Dual-X current conveyor differential input transconductance amplifier meminductor emulator circuit.

Thus, by combining(16) with (13):

$$\frac{V_{in}}{M_L} = g_m\left(V_{Z+}\right) \tag{20}$$

$$M_L = \frac{V_{in}}{g_m\left(V_{Z+}\right)} \tag{21}$$

Substituting (19) into (21).

$$M_L = \frac{V_{in}.M_R}{X_c.g_m.V_{X+}} \tag{22}$$

From (9), (14), and (15):

$$M_L = \frac{V_{in}M_R\left(sC_1\right)}{g_m V_{in}} \tag{23}$$

Hence,

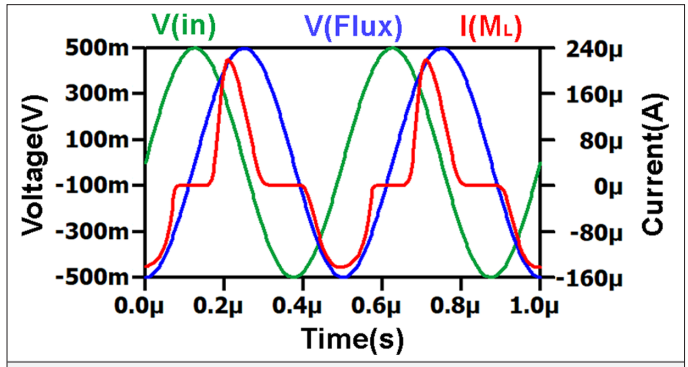

Fig. 5. Transient response of: (i) Input sinusoid, (ii) Flux, and (iii) Current I (M_L).

$$M_L = \frac{sC_1M_R}{g_m} \tag{24}$$

Upon substituting (14) into (24):

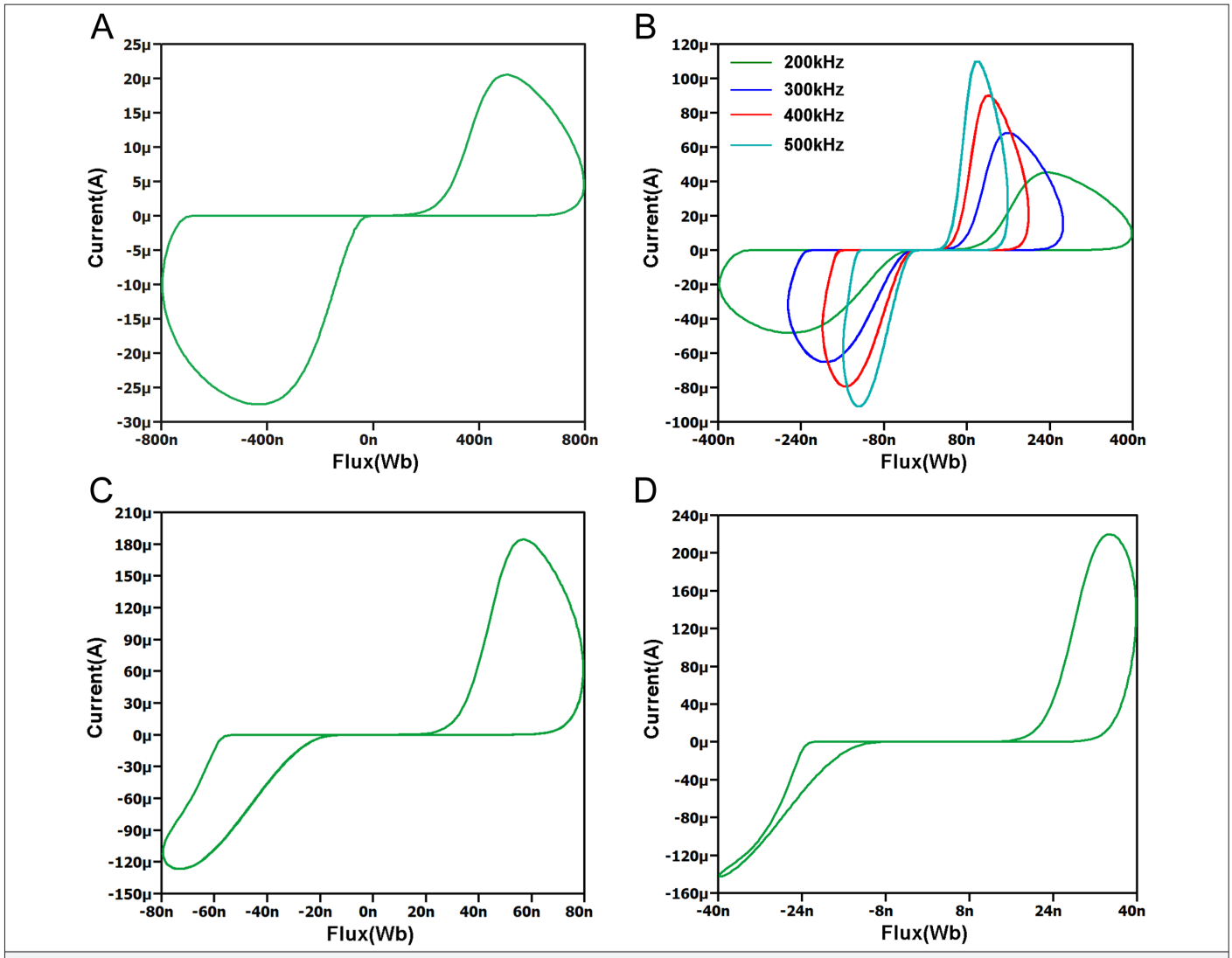

Fig. 6. V-I response of the meminductor emulator at different frequencies (a) PHL at 100 kHz. (b) PHL at 200 kHz to 500 kHz. (c) PHL at 1 MHz. (d) PHL at 2 MHz.

$$M_L = \frac{sC_1\left(\frac{1}{k\left(v_{c_2} - v_{in} - v_{tp}\right)} + \frac{R}{1+sRC_2}\right)}{g_m} \quad (25)$$

Upon further solving and rearranging, the impedance offered by the proposed meminductor emulator (M_L) can be derived as:

$$M_L = \frac{sC_1}{k\left(v_{c_2} - v_{in} - v_{tp}\right)g_m} + \frac{sC_1R}{\left(1+sRC_2\right)g_m} \quad (26)$$

From (26), it is evident that the meminductance is contingent upon both the capacitance (C_2) of the capacitor within the memristor emulator and the transconductance (g_m) of the DXCCDITA active block.

IV. SIMULATIONS RESULTS AND DISCUSSION

The operation of proposed meminductor has been simulated using the LTspice tool with the TSMC 0.18 µm model file for CMOS technology (Fig. 4). The bias current, denoted as I_{Bias}, is set to 50 µA, and the bias voltages are applied at ±0.9 V. The bias voltage (V_b) is fixed at 1 V, and the capacitor C_1 is set to 50 µF. In this context, C_2 and R of the memristor emulator are adjusted accordingly to achieve the required pinched hysteresis loop (PHL). The values are chosen as R=100 kΩ and C_2=100 pF, and the size of the PMOS has been adjusted to 10.8 µm/0.045 µm.

The first plot illustrates the transient response of the proposed meminductor to a sinusoidal input of ±500 mV for a frequency of 50 kHz. The transient plots for 1) V_{input}, 2) V_{Flux}, and 3) I_{ML} are presented in Fig. 5. The response demonstrates a phase lag between the current and the input voltage, as well as the flux. The pinched hysteresis loops are plotted in Fig. 6(a) and 6(b). The subsequent figure displays a variety of frequency plots from 100 kHz range to 2 MHz, demonstrating the unique properties of the meminductor devices. The effectiveness of the DXCCDITA-based meminductor has been confirmed across a broad range of frequencies by Fig. 6(a) and 6(b). The testing over this wide frequency range demonstrates the effectiveness across various applications, as stated previously. From the current vs. flux plot of the meminductor, it can be observed that as the frequency increases, the lobe area continuously decreases. The hysteresis plot also becomes pinched at only one value, which is at the origin. At zero frequency (DC), it remains at or approximately near the origin. This phenomenon serves as the distinctive signature of any memelement device. The proposed meminductor can support frequencies up to 2 MHz, and beyond this threshold, distinguishing the PHL plot becomes challenging. The power consumption of the device is found to be 203.887 µW.

A. Non-Volatility Test of Dual-X Current Conveyor Differential Input Transconductance Amplifier-Based Meminductor

The non-volatility test for the meminductor can be verified from Fig. 7. The test has been conducted using a pulse of 100 mV, which is tuned at a frequency of 50 kHz. The meminductor current retains a certain value even after the power is switched off, indicating that some value is sustained when the pulse is zero. With the arrival of a new pulse, the meminductor value continues to decrease, demonstrating its ability to learn and adapt to new values. Consequently, when there is no new information available to the meminductor, it achieves the final steady value according to the configuration.

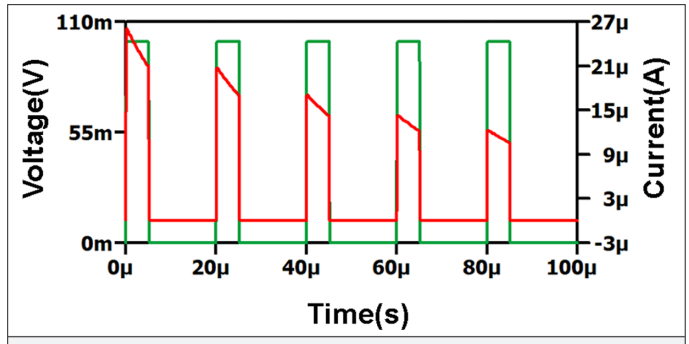

Fig. 7. Decremental meminductance M_L

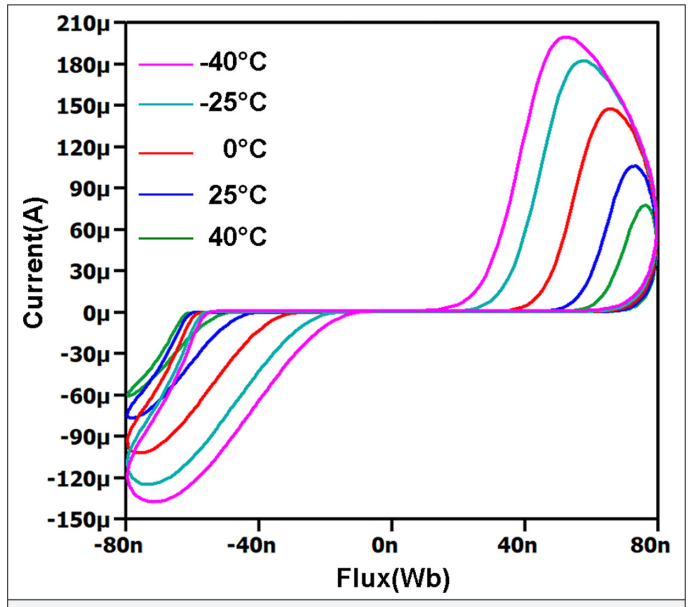

Fig. 8. Analysis of the meminductor's temperature within the range of –40 °C to 40 °C.

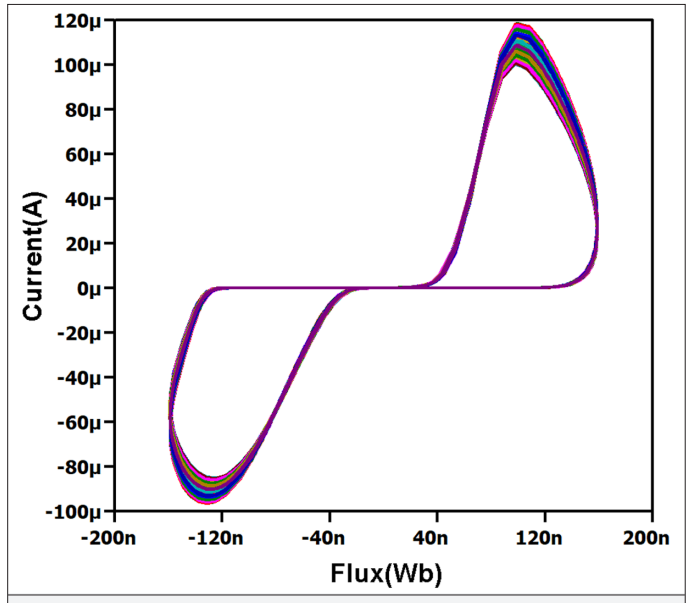

Fig. 9. Monte Carlo analysis at a tolerance of 5%.

The non-volatility test, as shown in Fig. 7, indicates that the meminductor processes the provided information and gradually reduces its capacity to retain unnecessary data, with performance assessed over time. This test confirms the signature of a meminductor element.

B. Temperature Analysis of Dual-X Current Conveyor Differential Input Transconductance Amplifier-Based Meminductor

Temperature analysis in a circuit is a critical aspect of ensuring reliable and efficient electronic performance. The operating temperature of electronic components directly influences their behavior, affecting

TABLE II. TABLE COMPARING THE PROPOSED EMULATOR WITH THE EXISTING ONE

Reference	Operative Elements	Static Components	Peak Frequency	Electronic Tunability	Floating(F)/ Grounded(G)	Power Dissipation	Technology Used
[6]	2 VDTA	2C	1.5 MHz	Yes	F	NA	CMOS 0.18 μm
[7]	3 OTA	2C	100 kHz	Yes	G	82.6 μW	CMOS 0.90 μm
[8]	2-DDCC+ 1-MOS	2R,1C	1.5 kHz	Yes	G	NA	CMOS 0.18 μm
[9]	1-VDTA+ 1-DOCCII	1R, 2C	200 kHz	Yes	F	NA	CMOS 0.18 μm
[10]	1-MVDCC + 1-OTA	1R, 2C	300 kHz	Yes	G	NA	CMOS 0.18 μm
[11]	2-OPAMP	1MR, 3R, 1C	5 kHz	No	G	NA	-
[12]	2-OTA+1-CDTA	2C	1 MHz	No	F	NA	CMOS 0.18 μm
[13]	1-OTA+1-CDBA+1-CCII	1R, 2C	1 MHz	No	G	NA	CMOS 0.18 μm
[14]	2-OPAMP	1MR, 4R, 1C	550 kHz	No	G	NA	CMOS 0.18 μm
[15]	2-CDTA	2C	500 kHz	No	G	NA	CMOS 0.18 μm
[16]	1-OTA+ 1-MOOTA	1R, 2C	1 MHz	Yes	F	3.87 mW	CMOS 0.18 μm
[17]	1-CCII+1-OTA	1MR, 1R, 1L, 1C	100 kHz	No	G	NA	CMOS 0.18 μm
[18]	1-VDBA+ 1-CDBA	1R, 2C	2 MHz	Yes	F	NA	CMOS 0.18 μm
[19]	1 VDBA	1MR,1C	4.9 Hz	Yes	G	NA	CMOS 0.18 μm
[21]	1-DOCCII+1-CCII	2R,2C,1L	700 Hz	No	G	NA	CMOS 0.35 μm
[22]	1-MVDVTA	1R, 2C	500 kHz	No	F	NA	CMOS 0.18 μm
[24]	1-OPAMP	1R, 1C	8 Hz	No	G	NA	-
[26]	2-CCII	1MR,1R,1C	24.1 Hz	No	F	NA	-
[39]	1-VDTA+ 2-MOS	2C	25 MHz	Yes	G	5.93 mW	CMOS 0.18 μm
[40]	1-OTA + 1 OPAMP	8R, 2C	5 kHz	Yes	F	NA	-
[41]	6-OPAMP	14R, 2C	3 kHz	No	F	NA	-
[42]	3-OPAMP	2R,2C	10 Hz	No	F	NA	-
[43]	VDCC	1MR, 1C	700 kHz	Yes	F	NA	CMOS 0.18 μm
[44]	1 CBTA	1MR, 1C	100 kHz	Yes	F	NA	CMOS 0.18 μm
[45]	4-CCII + 1-OPAMP	1MR, 1R, 1C	36.9 Hz	No	F	NA	-
[46]	1 OTA	1R, 1C, 1L	500 Hz	No	G	NA	-
[47]	2 OTA	2C	900 kHz	Yes	F	NA	-
[48]	1-OPAMP	1MR,3R, 1C	126 kHz	No	G	NA	-
Proposed	1DXCCDITA + 1MOS	1R, 2C	2 MHz	Yes	G	18.26 μW	CMOS 0.18 μm

CBTA, current buffered transconductance amplifier; CDBA, current differencing buffered amplifier; DDCC, differential difference current conveyor; DVCC, differential voltage current conveyor; MO-OTA, multiple output operational transconductance amplifier; MOS, metal oxide semiconductor; MVDCC, modified voltage differencing current conveyor; MVDVTA, modified voltage differencing voltage transconductance amplifier; TOA, transimpedance operational amplifiers; VDBA, voltage differencing buffered amplifier.

factors such as resistance, capacitance, and transistor characteristics. While conducting temperature analysis, Fig. 8 spanning from –40 °C to 40 °C, insightful observations have emerged from our simulations. Notably, there is a discernible trend where the area occupied by the hysteresis loop exhibits a consistent reduction as the temperature range increases. The decrease in the PHL lobe area implies a shift in the dynamic response of the circuit components, underscoring the impact of temperature variations on the overall performance. Such nuanced insights gleaned from our analysis contribute to a comprehensive understanding of the thermal characteristics of the circuit, facilitating informed design decisions and enhancing the proposed circuit's resilience across a broad range of operating temperatures.

C. Monte Carlo Analysis

The influence of transistor discrepancies and overall process fluctuations on the proposed meminductor emulator has been explored in Fig. 9, which displays the outcomes of a Monte Carlo analysis. The simulations, conducted 200 times, reveal a slight modification in the pinched hysteresis loop of the memristor circuit layout. Nevertheless, the overall operation remains within permissible boundaries. Significantly, it is worth noting that, in every Monte Carlo iteration, the flux-current curves consistently intersect the zero point. It is important to highlight that the simulations have been executed on capacitor C_2. Consequently, the level of tolerance for the variable has been appropriately adjusted to 5%. The efficacy of our suggested meminductor circuit has been successfully verified through this comprehensive analysis, leading to new opportunities for circuit design and functionality.

D. Comparison of Proposed Emulator With Available Emulators

In this segment, an evaluation of the principal specifications of the proposed meminductor emulator is conducted in conjunction with previously documented structures found in recent publications. The results of the comparative analysis are compiled and presented in Table II. The main variables utilized for the intention of this juxtaposition comprise the count of dynamic and dormant constituents, the scope of favorable high-level signals frequency, the indispensability of integrating a memristor in the blueprint, electronic adjustability, and the adaptability to the manners of functioning. From the table, it becomes apparent that the proposed meminductor emulator in this study has distinct characteristics. By moving away from the traditional reliance on multiple building blocks [6-18, 26, 40-42, 45, 47], proposed meminductor makes it possible to use only a single DXCCDITA active block. Moreover, the proposed meminductor emulator design distinguishes itself from prior designs by the omission of a memristor in its implementation [11, 14, 19, 36, 43-45, 48]. The utilization of a memristor emulator has provided us with the capability to fulfill essential frequency prerequisites, an accomplishment that was previously unachievable with circuits employing the presently accessible memristor. In light of this advancement, we have been able to overcome the limitations imposed by traditional memristor-based circuits and effectively address the critical demands of frequency specifications. The omission of multiplier circuit blocks [8, 16, 21, 40-41] have reduced complexity and enhanced the performance of the meminductor circuit. The table further imparts to us an understanding that despite the exclusion of intricate circuitry and memristor, the meminductors in question manage to attain a frequency of a few hundred kilohertz except [18, 39], whereas the proposed meminductor expounded upon in this manuscript achieves a frequency range of 2 MHz. In contrast to the fixed characteristics of meminductors highlighted in the references [7-11, 14-19, 21-22, 24, 26, 40-47], the

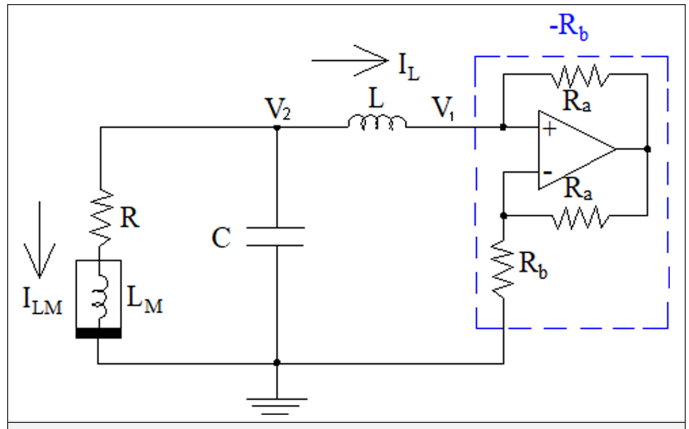

Fig. 10. Circuit of Chua's chaotic oscillator.

proposed meminductor circuit provides inherent electronic tunability, as evidenced by (13). This equation serves as a validation that the proposed meminductor can be tuned using only two components: the bias current I_{bias} and the voltage across the terminals V_Z. This flexibility is a key feature of our meminductor design.

E. Chua's Chaotic Oscillator: The Application of Proposed Meminductor Circuit

Chaotic oscillators are well-known devices operating in various fields such as physics, biology, and economics [49]. They are primarily characterized by irregular, random motion, making them highly unpredictable over extended time periods. Examples include analyzing complex and nonlinear dynamics in fluid physics, secure communications in fields like banking, trading, security, cryptographic techniques, and data encryption algorithms. In Chua's chaotic oscillator circuit illustrated in Fig. 10, an inductor (L), capacitor (C), and a resistor (negative) have been incorporated, alongside a non-linear element. In our simulations, we have substituted the nonlinear element with the proposed DXCCDITA-based meminductor. The performance of the chaotic oscillator has been verified for various components. The 2D projection plots with their sinusoidal outputs have been showcased in Figs. 11 and 12. These figures unequivocally confirm the chaotic behavior exhibited by a meminductor

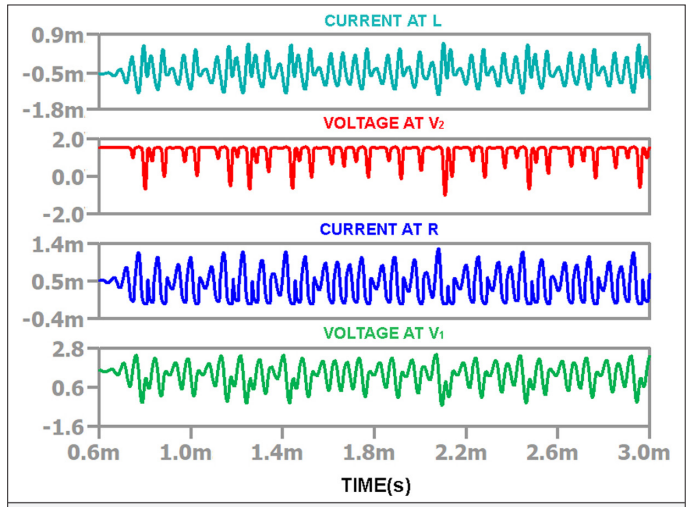

Fig. 11. Response of chaotic oscillator circuit.

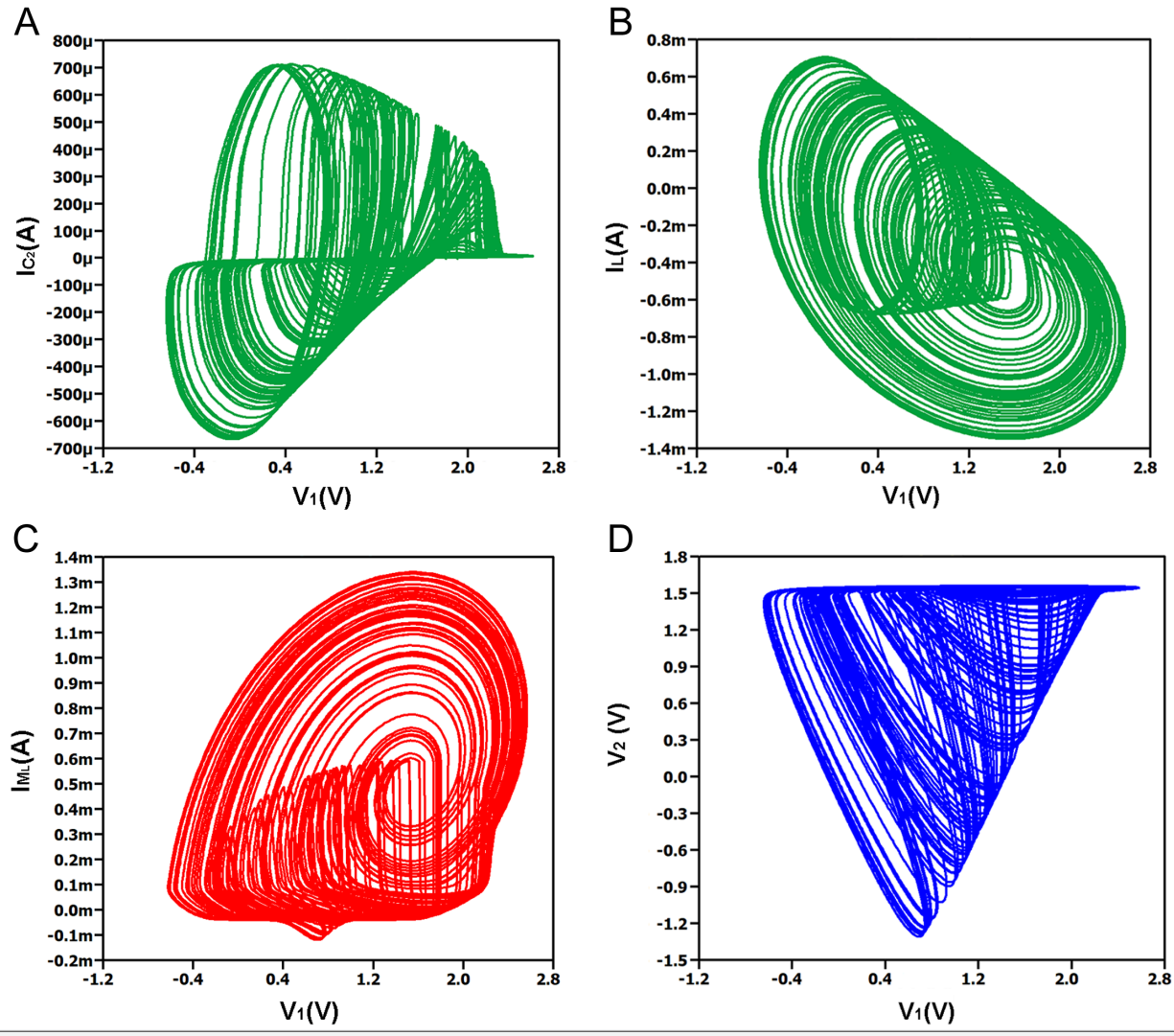

Fig. 12. Different plots corresponding to varying voltage and current sources (a) I_{C2} vs V_1. (b) I_L vs V_1. (c) I_{ML} vs V_1. (d) V_2 vs V_1.

device, thereby affirming its suitability for a wide array of applications such as Random Number Generators (RNGs), Pseudo-Random Number Generators (PRNGs), encrypted communication, and neuromorphic circuits. The simulations were performed using resistor values of R_a, R_b, and R set to 10 Ω, 3 kΩ, and 10 Ω (internal resistance of the meminductor), respectively. The capacitor C was adjusted to 2.3 nF, and lastly, the inductor was tuned to 14 mH. Various plots are displayed in Fig. 12, demonstrating the chaotic behavior across the components, encompassing different voltages and current components.

V. CONCLUSION

This research introduces a grounded meminductor emulator incorporating a DXCCDITA, a grounded memristor emulator, and a capacitor. The circuit proposed in this study offers a distinct benefit compared to the currently existing meminductor emulators, thus emphasizing its independence from analog elements and its improved capability for adjustments. The meminductor demonstrates significant and robust support across a wide frequency range from 100 kHz to 2 MHz, as validated through PHL and non-volatility testing. Reliability assessments, including temperature analysis and Monte Carlo simulations, further underscore the circuit's robustness. Validation through support of a chaotic oscillator underscores its real-time usability, laying the groundwork for future advancements in meminductor-based circuits.

Availability of Data and Materials: The data that support the findings of this study are available on request from the corresponding author.

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Author Contributions: Concept – S.K.R.; Design – A.C.; Supervision – K.S., S.S.; Resources – A.C., K.S.; Materials – A.C., S.K.R.; Data Collection and/or Processing – A.C., S.K.R.; Analysis and/or Interpretation – A.C., S.S.; Literature Search – A.C., S.K.R.; Writing – A.C.; Critical Review – K.S., S.S., S.K.R.

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