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Ultra Wideband High-Efficiency High-Power Amplifier Design by Simplified Output Matching Technique

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ABSTRACT

This paper presents the design of a Gallium Nitride (GaN) transistor-based ultra-wideband (UWB) high-efficiency power amplifier (PA) with 25W (44 dBm) output power operating in the 2–6 GHz frequency band. The design of the matching circuits is based on a simplified systematic approach utilizing the target impedance trajectory. The Macom CGHV1F025S model GaN transistor and Rogers RT5870 model substrate are used in the design. The experimental results show that performance of the implemented PA offers 9.8 dB power gain, 43.8 dBm output power, and power-added efficiency (PAE) between 41% and 57% in the 2–6 GHz band.
***Index Terms*—**Gallium Nitride (GaN) (HEMT), high power, high-efficiency power amplifier, wideband power amplifier

I. INTRODUCTION

Radars, electronic warfare systems, and communication systems use power amplifier (PA) system modules to generate signals with broadband characteristics and then transmit them over long distances. These systems operate in their allocated frequency bands [1, 2]. For example, a jammer device can be used to prevent communication between 1 GHz and 6 GHz. As another example, in 5G communication systems, many frequency bands below 6 GHz are available for communication. Designing a separate device for each band would cause design, manufacturing, and cost problems for users, designers, and vendors. For those reasons, wideband is being preferred in PA design. With wideband design, high-efficiency structures are tried to be designed in order to reduce operating costs and extend the product life. Providing these two parameters together requires some new approaches. In a PA with high output power, the heat generated in the transistor which is the active element, must be removed from the environment. Moreover, in high-power operation, the transistor requires a high supply voltage. Therefore, both facilitating thermal management and minimising the need for high supply voltages in the system are possible by operating the high efficiency of the PA.

In order to increase the bandwidth of the PA while maintaining high efficiency, several methods are available in the literature, such as the reactance compensation technique [3], the low-pass matching technique [4] and the real frequency technique [5] and [6]. However, the first 2 of these techniques are difficult to realize over an octave bandwidth. Distributed-parameter PAs can contribute to solving this problem. However, due to limitations such as low gain, low efficiency, and relatively large structure size, they are difficult to be widely applied. Considering the need for a wideband, high-efficiency PA in these systems, the design of a PA that meets these specifications is the main subject of this work.

In this article, the sections will proceed as follows: firstly, the source pull (SP) and load pull (LP) analyses of the used transistor is performed in detail. Then, the input matching network (IMN) and output matching network (OMN) of the 25W PA is designed by the N-section stepped impedance matching technique. The synthesized impedances of the matching networks are tried to be placed close to the target impedance region obtained from the SP and LP. Then, the overall PA structure is constructed with bias networks and IMN/OMN. Finally, the fabrication of the PA and the experimental results of the 25W PA are discussed.

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II. WIDEBAND (2–6 GHZ) 25W POWER AMPLIFER DESIGN

In this section, the design of a high-efficiency PA operating in the 2–6 GHz band with an output power of 25 W is presented. Macom CG2HV1F025S model transistor is used in the design. After verifying the model, the bias voltages at which the amplifier operates are determined. At the determined gate and drain bias voltages and input powers, SP and LP analyses are performed in the desired frequency band. Target impedance regions for IMN and OMN are defined by considering the P_{out} and power-added efficiency (PAE) contours obtained as a result of SP and LP analyses. As a result, it is aimed to place the input port (gate side) impedances of the synthesized IMN and output port (drain side) impedances of the OMN in these target regions.

A. Determination of the Bias Points

The I–V output curves of the transistor are given in Fig. 1. The point at which the transistor is biased (in the operating class) is determined by considering the trade-off between the efficiency–bandwidth –harmonic distortion relationship. The bias point is determined so that the efficiency value is around 50% and the harmonic level is sufficiently low within the operating band. Thus, V_G:-2V and V_D:30 V are chosen.

B. Source Pull–Load Pull Analysis

In small-signal operation, the maximum power transfer approach (conjugate matching) is taken as a reference in amplifier design. However, in large-signal operation, the maximum power transfer theorem, although useful in the design of the input stage (circuit), is largely not used in the design of the output circuit of an amplifier. Instead, it is designed to deliver a certain amount of power to the load, and then the efficiency, gain, and linearity are evaluated (and the design iterated if necessary) to see if they are within the desired values. SP/LP analysis is performed to transfer the desired amount of power to the load.

Source pull and LP are design technique in which the source and load impedances presented to a transistor are varied by an impedance tuner to find the optimum input and output impedance values to obtain the desired performance from the PA. By presenting varying load and source impedances to the PA, the aim is to obtain the output power and efficiency contours on the Smith chart for defined frequencies.

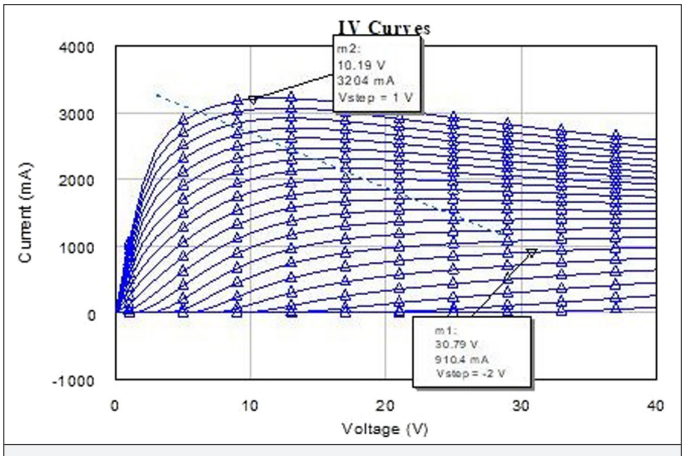

Fig. 1. I–V output curve of CG2HV1F025S transistor.

Let us consider how to design the matching circuit to be placed between the output transistor and the load. As shown conceptually in Fig. 2 (a), through a lossless variable passive (can also be active) circuit (a "tuner"), the complex and real impedance components are externally controlled so that the load impedance Z_1 is the impedance from the output of transistor M_1 to the load. The impedance Z_1 is varied so that the power delivered to R_L remains constant and equal to P_1, resulting in the constant P_1 contour shown in Fig. 2 (b). The P_1 contour at low power corresponds to a wider range of Re{Z_1} and Im{Z_1} and therefore a wider contour. Analysis continues to then search for Z_1 values to obtain another (perhaps more narrowly spaced) contour, which provides a higher output power P_2. These LP measurements can be repeated as power levels increase, finally reaching the optimum impedance, Z_{opt}, for maximum output power.

In the above SP/LP setup, the input impedance Z_{in} of the transistor is relatively dependent on the value of Z_1 due to the gate-drain capacitance of M_1. Therefore, the power delivered to the transistor varies with Z_1, leading to a variable power gain. This effect can be avoided by placing another tuner between the signal generator and the gate and adjusting its impedance to achieve conjugate matching at the input for each value of Z_1 (Fig. 2 (c)). However, in a multistage PA, this tuning may not be very necessary because after Z_1 reaches its optimum value, Z_{in} settles to a certain value and the previous stage is generally designed to drive the Z_{in} load.

The SP/LP setup is shown in Fig. 3. HBTUNER element is used to adjust different impedance values at the input and output sides of the circuit. With this tuner, the fundamental frequency, second- and third-harmonic impedances can be adjusted separately. In addition to the impedance values, other parameters such as bias voltage, operating frequency, and input power can be adjusted simultaneously in the SP/LP test structure so that a detailed analysis can be performed. In order to determine the optimum source and load impedances for the desired output power and PAE, the analysis was performed at 500 MHz intervals between 2 GHz and 6 GHz. Since the impedance values of transistors vary with different input power levels and bias voltages, SP/LP analysis should also be performed for a given input power level and bias voltages to obtain appropriate impedance values. In this work, the input power level and gate and drain voltages for the SP/LP simulations are 34 dBm and –2V/30V, respectively.

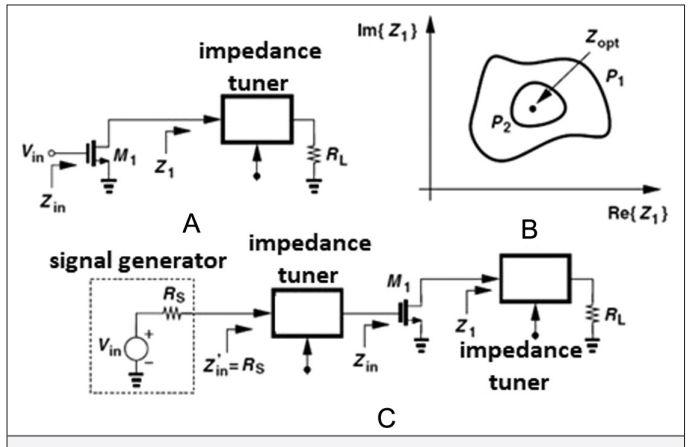

Fig. 2. Load-pull analysis circuit (a), contours obtained by load-pull (b), and a measurement setup for determination of impedances of input–output matching circuits (c).

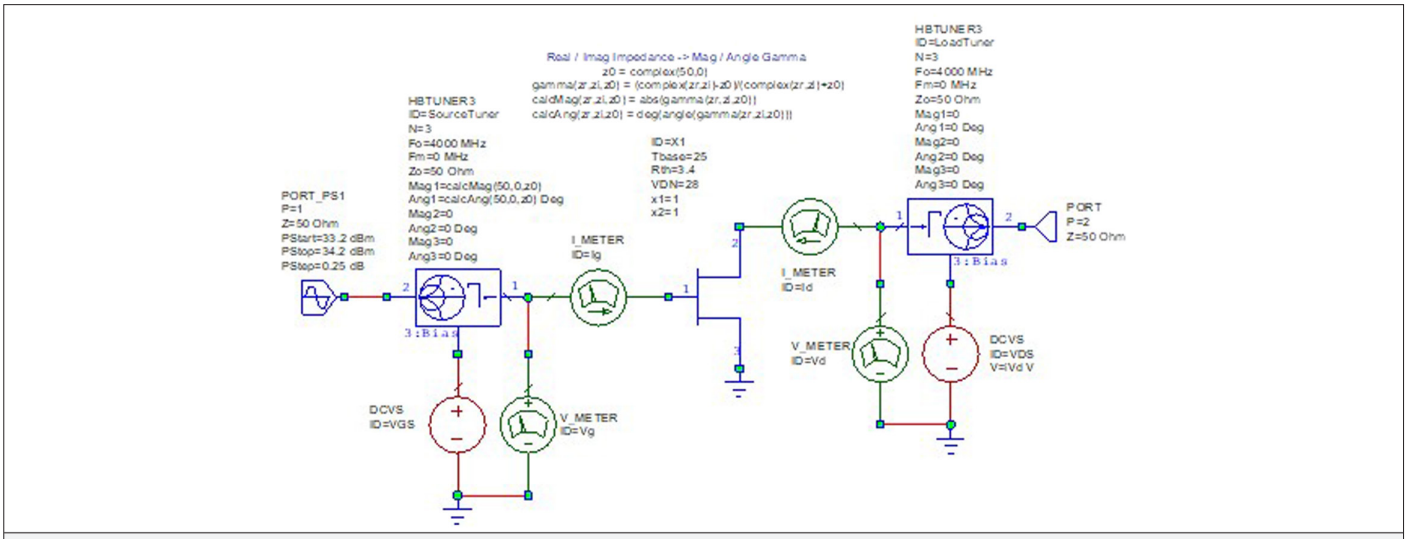

Fig. 3. SP/LP analysis setup.

Source pull/LP test setup in Fig. 3, impedances (or reflection coefficients) can be determined in one go with nested measurements for the load and source sides. For example, if the firstharmonic is selected on the source and load sides for SP/LP analysis (Fig. 4), these two measurements are nested and produced as a single load-source pull output file.

Source pull contours for f: 2, 3, 4, 5, and 6 GHz according to the selected source-load impedances are given in Fig. 5. According to the data obtained from the source pull analysis, 43.5 dBm output power and 50% PAE are targeted in line with the design goal. Fig. 5 shows the contours providing 43.5 dBm output power and 46% PAE for SP.

The reflection gamma points obtained from the design of the input matching circuit are intended to be located in the regions selected in this target region (see Fig. 5). Similarly, as a result of the LP analysis, the OMN is designed according to the targeted impedance set

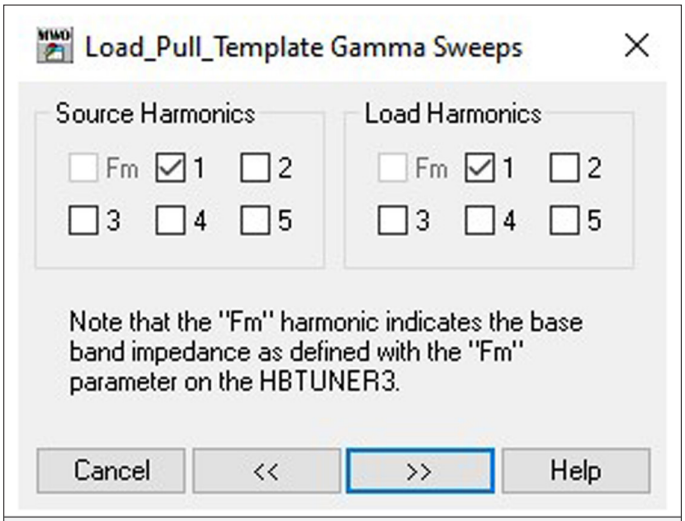

Fig. 4. Selecting "nested" analysis to determine the source and load impedances at fundamental frequencies for SP/LP analysis.

in the intersection region of the contours providing 43.5 dBm output power and around 50% PAE for the 2–6 GHz band. As can be seen from Fig. 6, the output power is around 44 dBm and the PAE is around 60%.

As a result of the SP/LP, it is seen that the impedance region achieving the desired output power and efficiency at the desired bandwidth is distributed over a wide area. Using this impedance region, IMN and OMN were designed in the closest possible regions to the targeted impedance locations.

C. Systematic and Simplified Design of Input Matching Network and Output Matching Network

A simplified systematic approach for the design of matching circuits is presented, referring to existing techniques such as the N-section transformer and stepped impedance technique [7 and 8]. To illustrate the considerations in the presented simplified approach, the variation of the output impedance of the transistor with respect to frequency at a given bias point is depicted. At V_G:-2V, V_{DS}:30V bias voltage, R_{out} = 12.5 Ω and C_{out} = 1.56 pF for f_0:3.2 GHz.

$$BW \le \frac{1}{2R_{opt}C_{out}\ln\left|\Gamma_L\right|^{-1}} = \frac{\pi f_0}{Q_{opt}\ln\left|\Gamma_L\right|^{-1}} \quad (1)$$

$$TPG = \frac{\left|S_{21}\right|^2\left(1-\left|\Gamma_L\right|^2\right)}{\left|1-S_{22}\Gamma_L\right|^2} \quad (2)$$

As shown in Fig. 5, the source impedance of the transistor for maximum P_{out} and PAE is on the border of short circuit region. Therefore, the impedance transformation ratio between the source and 50 Ω terminal impedance is very high. Such a huge impedance transformation ratio makes impedance matching very difficult. This is why an impedance region is aimed for both to be easily transformed to 50 Ω and power gain of 9.5 dB in the bandwidth. Hence, the impedance region of the IMN is in the selected region as demonstrated in Fig. 5. The "Input_matching_Zin1" (see Fig. 5) of the synthesized IMN is near the target impedance trajectory. The IMN design is based on a trade-off between low input reflection and gain flatness, taking into account Pout and PAE performance.

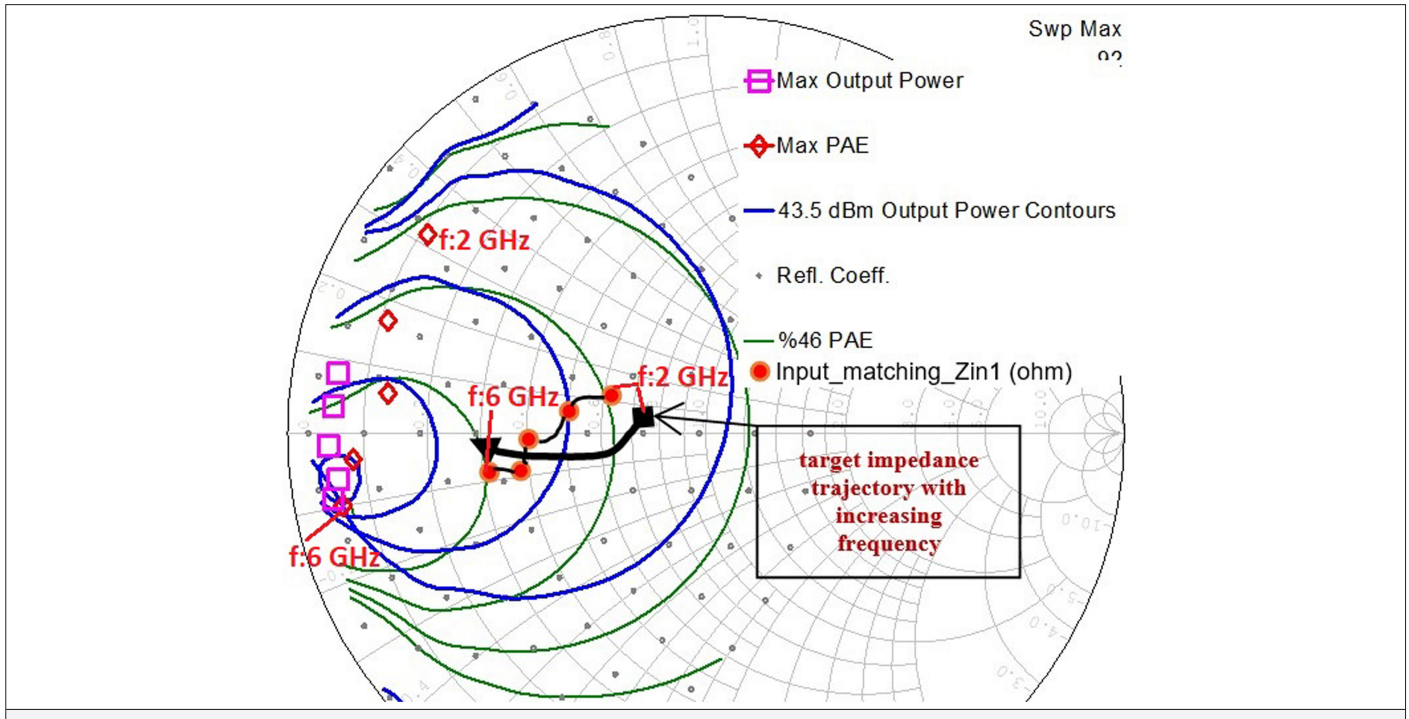

Fig. 5. The placement of the optimal impedance points and giving the maximum output power (pink square box) and maximum PAE (red box) of the transistor as a result of the SP.

In-band stability is ensured by the R-C structure in series parallel to the gate; low-frequency stability is provided by the gate bias resistor [11].

In the OMN design, the intersection of the 37.8 dBm P_{out} and 45% PAE contours is targeted for both P_{out} and PAE performances. In the OMN designs, an optimization is usually performed for the target parameters. However, this optimization method generally takes a long time, and also a convergence problem may arise. Therefore, initial values of the components of the IMN and OMN must be determined by using systematic steps and methods.

Since the design is wideband, several important factors need to be considered to achieve the desired performance (such as gain flatness, efficiency, harmonic level, etc.). For example, if gain flatness is desired, the gain behavior of the transistor in the frequency range of interest will be important. Here, an N-section transformer-based Chebyshev lowpass network approach has been preferred in the

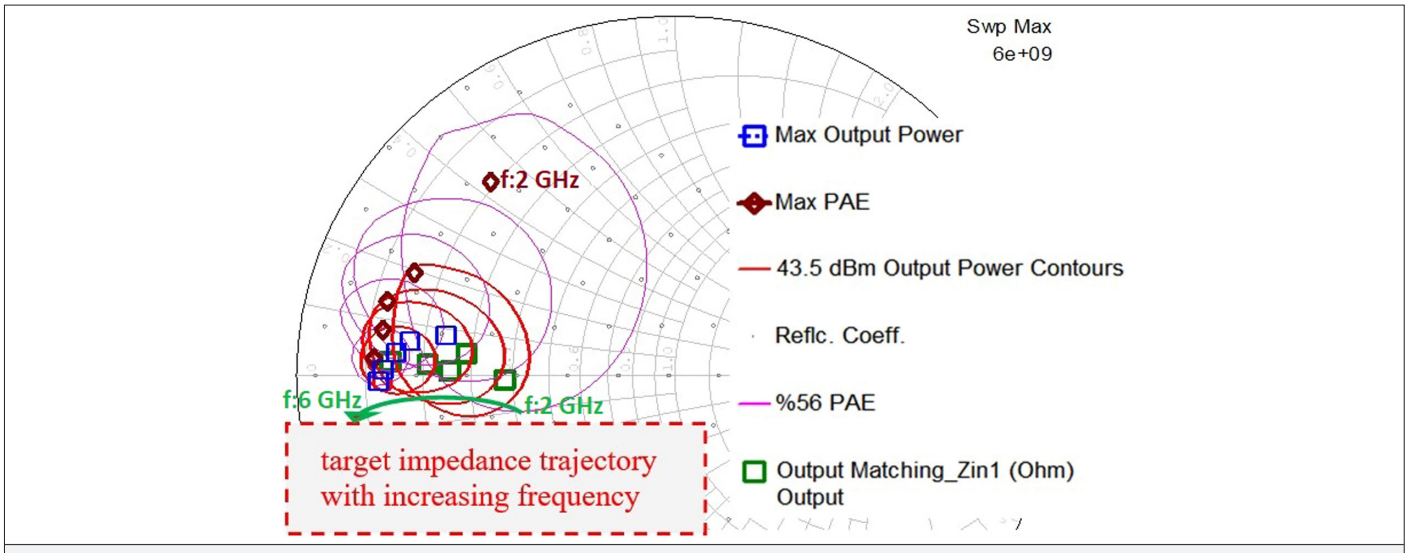

Fig. 6. The placement of the optimal impedance points and input impedances of the output matching circuit (green square box), giving maximum output power (blue square box) and maximum PAE (brown box) as a result of LP of the transistor.

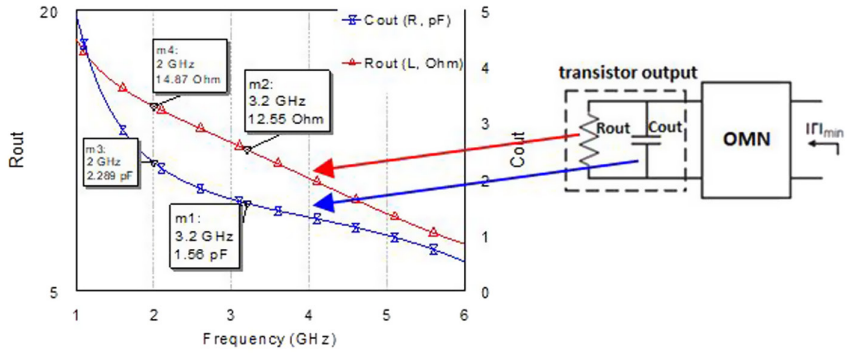

Fig. 7. R_{out} and C_{out} curves with respect to frequency and a representative model of the output impedance of any transistor.

matching network design. The design procedure is briefly explained as follows:

- The matching band is considered as two frequency regions since the gain behavior of the transistor is not flat within the band.
- The source/load-pull of the used transistor is performed.
- The desired parameters, including the center frequency f_0 (in our design, especially f_0:4.5 GHz to compensate lower gain of the 3 GHz < f < 6 GHz region compared to 2 GHz < f < 3 GHz frequency region) and the operating bandwidth, are set.
- The complex impedance of the gate (R_{gate}+C_{GS}) to 50 Ω and the complex impedance of the drain (R_{out}//C_{out}) to 50 Ω conversions are done [9].
- The order of the lowpass matching network is determined by the step-by-step tuning method.
- The lumped LC element values of the low-pass transformation network can be calculated using equations in [10].
- To realize the LC ladder in microstrip form, a straightforward conversion from LC to stepped impedance microstrip lines is applied [8].
- The initial values of the stepped impedance network in microstrip form are calculated [10].

The AWR Microwave Office program has a "stepped()" function feature used to discretely tune and optimize variables. With this function, it was ensured that optimization was done only in certain steps in the desired region without using the optimization program. Without discrete optimization, transmission line length/width values can be assigned unrealistic (unrealizable) values, for example, a transmission line width of 0.05 mm for our printed circuit fabrication device. This discrete stepped approach allows the values to be assigned discrete and realizable. The lengths and widths of the filter can be tuned and optimized over a range of discrete values defined by the stepped functions in AWR (shown below).

Length = stepped (1, 20, 0.1) (in mm)

Width = stepped (0.2, 10, 0.1) (in mm)

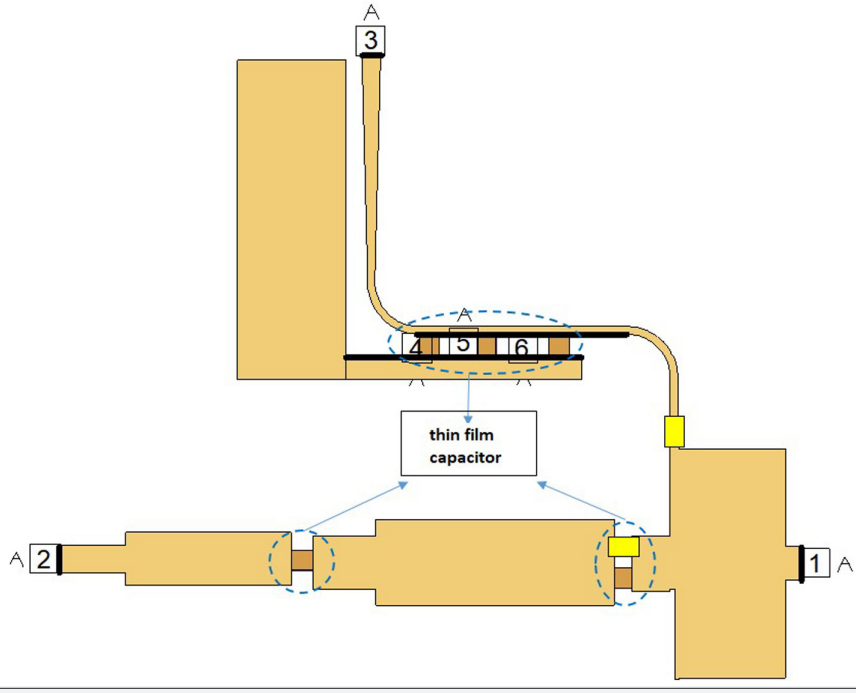

Fig. 8. EM simulation circuit layout of the input matching network together with the bias line.

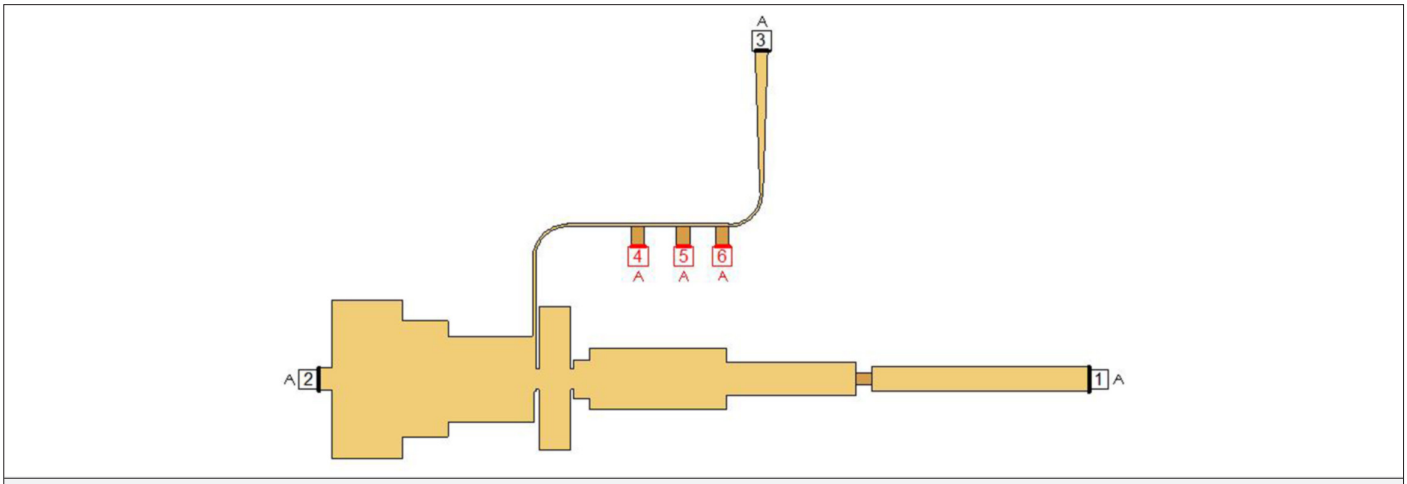

Fig. 9. EM simulation circuit layout of the output matching network together with the bias line.

In this regard, in view of the aforementioned considerations, an optimizer's goals are set [11]. Firstly, the transducer power gain (in (2)) of the IMN is aimed for −3 to 0 dB for 2–3 GHz, and −1 to 0 dB for 3–6 GHz to provide gain flatness [5, 10]. Moreover, the Q factor corresponding to the output impedance ($R_{opt}//C_{out}$) of the transistor is ~30% higher in the 2–3 GHz band than in the 3–6 GHz band (see Fig. 7). Hence, according to (1), for a frequency region with a higher Q, low return loss performance is preferred to realize a more convenient wideband matching design [9].

D. Realization of EM Simulation for Before Fabrication of the Designed Power Amplifier

Before fabrication, an EM simulation is performed to identify realistic situations that cannot be seen in the schematic simulations, such as indentations of the transmission lines, EM radiation at transitions between the lines, etc. Otherwise, re-production may be necessary to modify unexpected results. The layout of the IMN is shown in Fig. 8. For the representation of the shunt capacitors on the supply line and coupling capacitors on the signal line in the schematic circuit, a thin

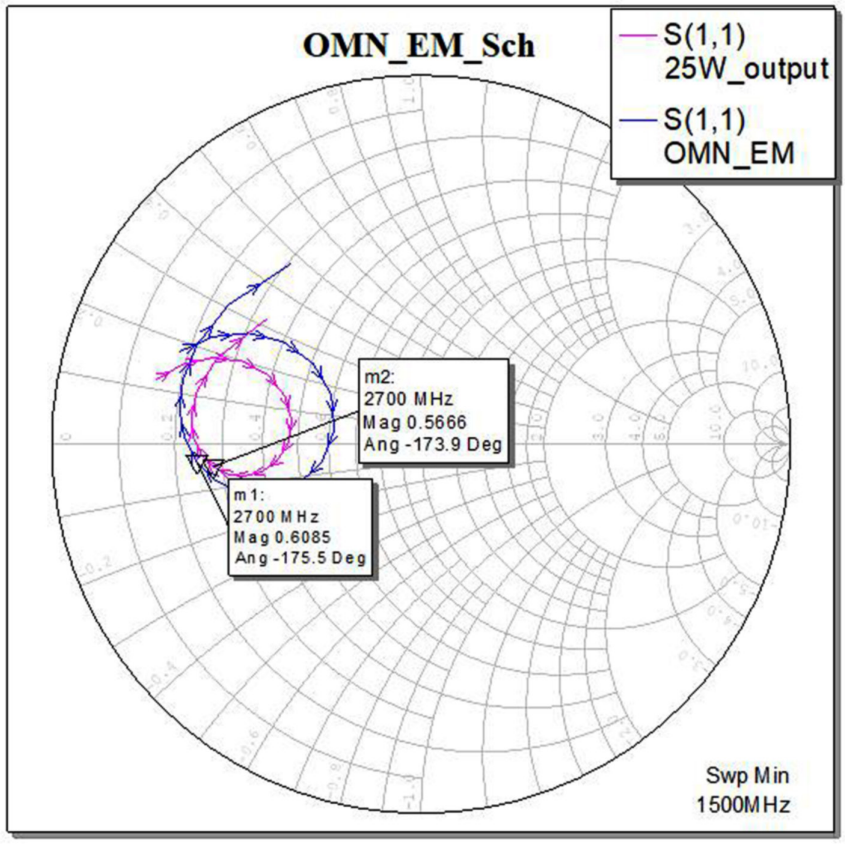

Fig. 10. Demonstration of the impedance trajectory obtained by the schematic and EM simulation of the output matching network.

film capacitor element is used in the EM simulation circuit. The placement of these capacitors in the EM simulation is expressed as labeled with numbers. In Fig. 8, port 1 shows the gate terminal; port 2 shows the output connector terminal; and ports 4, 5, and 6 show the capacitor connection parts to be soldered to the bias line.

The layout of the OMN prepared for EM analysis is shown in Fig. 9. Here, port 2 shows the drain terminal; port 1 shows the output connector terminal; and ports 4, 5, and 6 show the capacitor connection parts to be soldered to the bias line.

After EM simulation of the S-parameters of the OMN with respect to frequency, it is seen that there is some difference between the schematic simulation and EM simulation results. This difference in impedance values (S-parameters) can be seen in Fig. 10.

The deviation of the impedances obtained from the schematic and EM simulations in the 2–6 GHz frequency band in certain regions is improved by optimizing it in several steps. Since the EM simulation takes a long time, the smallest change in each optimization step takes time. Therefore, the lines are readjusted so that the changes can be completed in as few steps as possible. After optimization, the schematic and EM-simulated gamma points are close to each other, as can be seen in Fig. 11. Thus, the OMN is in its finalized form.

III. FABRICATION OF 25W POWER AMPLIFIER AND EXPERIMENTAL RESULTS

The designed 25 W PA is fabricated on a Rogers RT 5870 model substrate. A copper plate, on which the base of the fabricated PA is placed, is also prepared by sizing the copper plate. The purpose of the copper plate is to enhance the cooling of the circuit by increasing heat conduction and to increase the robustness of the circuit board (as shown Fig. 12).

The most important issue to be considered before starting the measurements is the bias sequence of the active element GaN transistors. Since GaN HEMT transistors are depletion mode, the channel is active and conducts even at 0V gate voltage. Before connecting the drain supply (before activating it), a certain sequence must be followed to avoid damaging the transistors: Before starting the measurement, all supply connections must be made with the power supplies switched off. When the measurement is started, the currents of the power supplies must be limited to their respective limit values in order not to damage the circuit.

Another important issue before starting the measurement is the calibration of the test bench. Losses and effects caused by each device and cable used in the measurement should be determined and excluded from the measurement results of the main system (device under test) being measured. For the calibration of the measurement system, the calibration setup in Fig. 13 is set up. Calibration is performed for the relevant input powers and specific frequencies, and the resulting values are noted. Thus, the PA circuits under test are measured with higher accuracy (Fig. 13).

After the calibration is completed, the connections of the 25W PA are performed for measurement (see Fig. 14). One of the important points here is that the RF cable connector and the

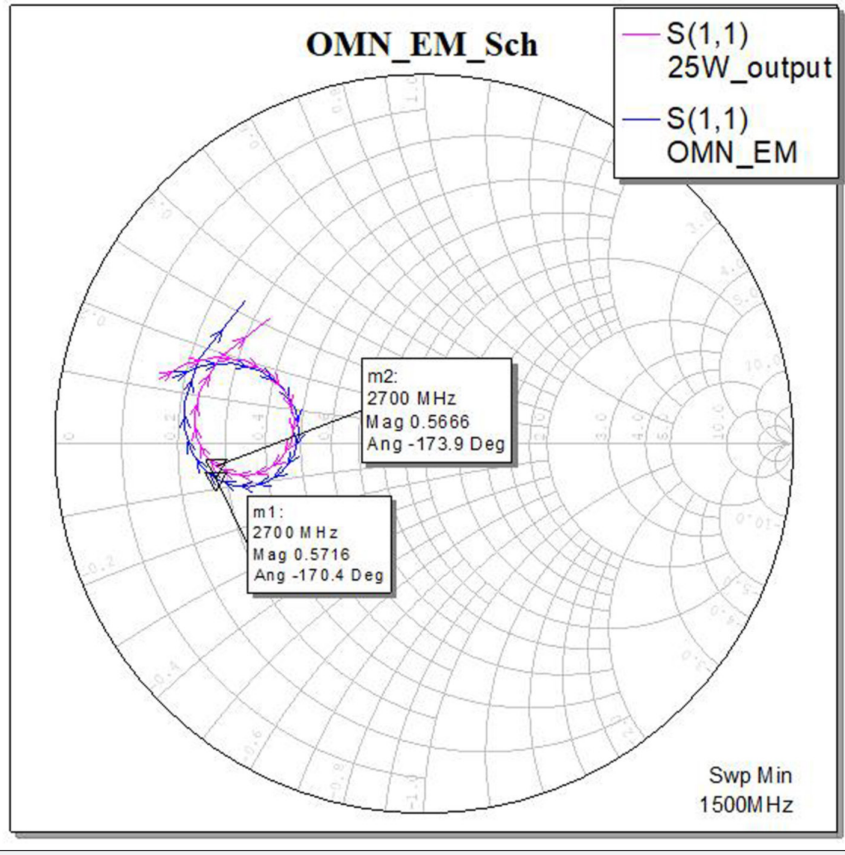

Fig. 11. After optimization, demonstration of the impedance trajectory obtained by the schematic and EM simulation of the OMN.

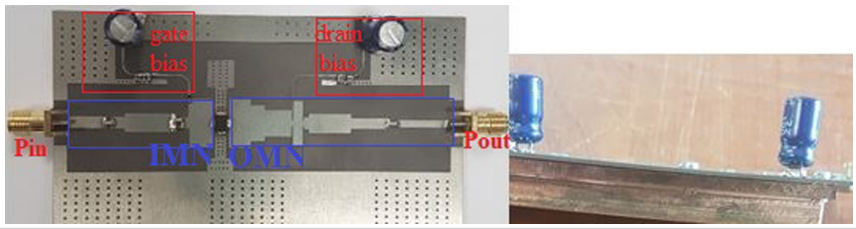

Fig. 12. The fabricated 25W PA (left) and the copper layer added under the board for cooling and durability (right).

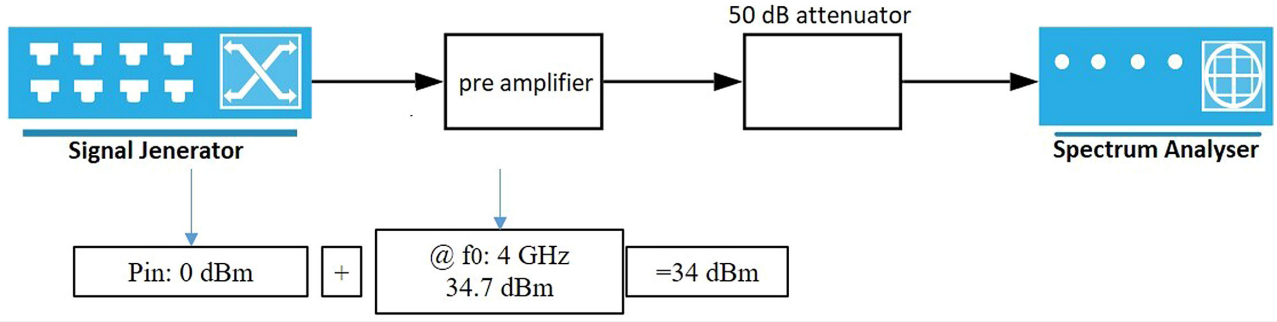

Fig. 13. Representation of the calibration setup.

circuit connector must be fully connected so that there is no reflection. Therefore, the connection should be checked with a torque wrench. After the test setup is established, small signal simulations are performed first. Then, the output power for each frequency was measured at 100 MHz intervals in the 2–6 GHz frequency band. When an input power of P_{in}:34 dBm is applied to the input of the 25W PA at f_0: 4 GHz, the output power seen on the spectrum analyzer is -5.7 dBm as depicted in Fig. 15. Since there is a 50 dB attenuator at the output of the 25W PA, P_{out} is calculated as follows: $P_{out=}$ 34 dBm (P_{in}) + 9.7 dB (Gain) – 49.5 dB (attenuator) ≈ -5.7 dB. The resulting measurement data is shown in Fig. 16 together with the simulation data.

The results in Fig. 16 show that the output power in the operating band is 44.2 dBm–43.4 dBm, the gain is 10–9.32 dB, and the PAE is between 41% and 57%. –

The measurement to examine the output power with the variation of the input power is presented in Fig. 17. At f_0: 4 GHz, frequency between 20 dBm and 40 dBm input power are swept, and a 1-dB

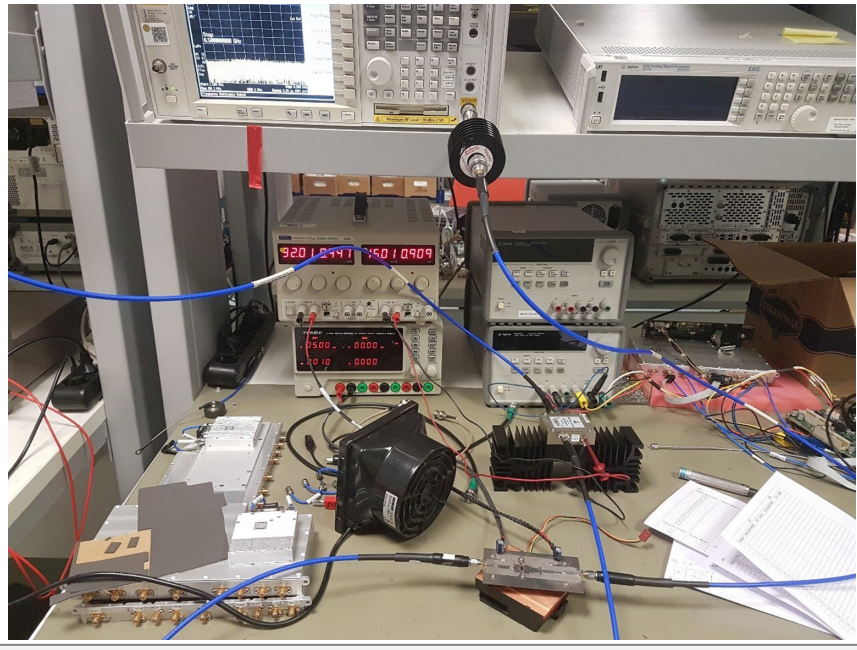

Fig. 14. Measurement setup of the 25W PA.

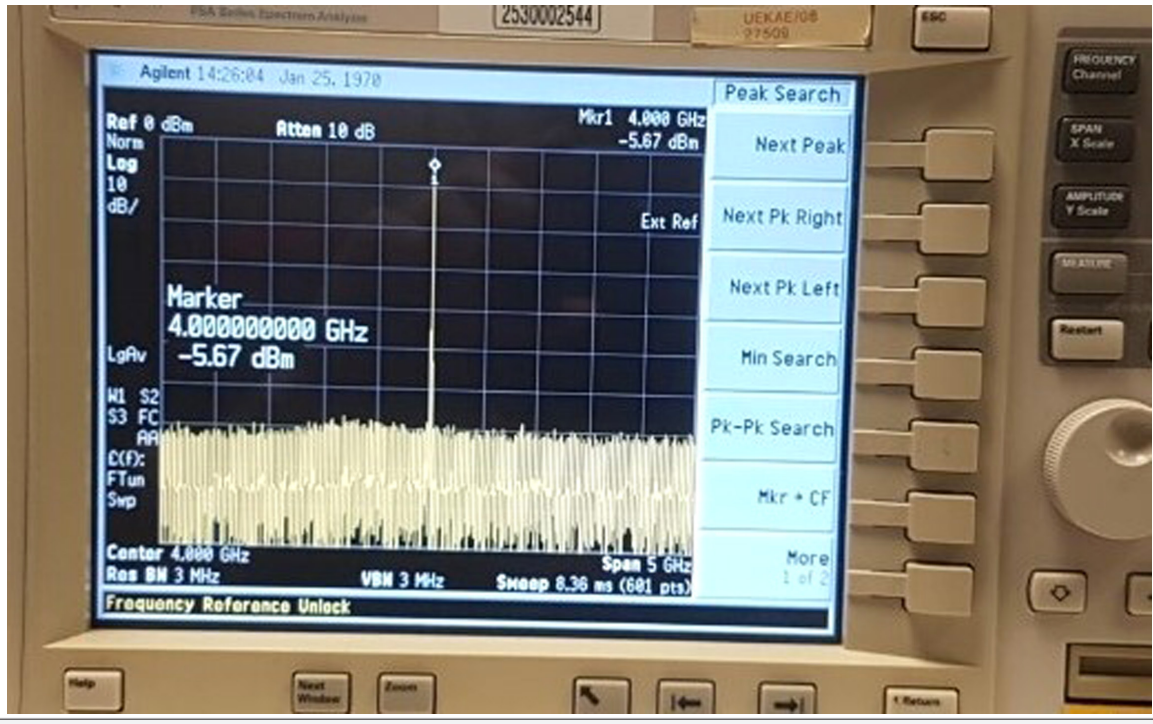

Fig. 15. Output power spectrum for P_{in}=34 dBm input power at f_0:4GHz frequency.

compression point is detected. From about a 30 dBm input power level upwards, linearity starts to degrade and PAE also decreases.

Finally, for some frequencies, the harmonics in the output power spectrum are analyzed with a one-tone signal test. Fig. 18 shows the harmonic measurement results of the 25W PA. At f_0: 4 GHz, the second harmonic is 34 dB lower than the fundamental signal; at f_0: 5 GHz, the second harmonic signal is 30 dB lower than the fundamental signal.

The performance parameters of the experimental results are given in Table I. In addition, similar studies in the literature are summarized in Table I.

*FOM (1K) defines 1000 times the column value. A figure of merit (FOM) is defined to compare the studies. The defining FOM = Fractional BW (%) × Upper limit of the band (GHz) × P_{out} (W) × PAE (%) × Gain (dB). Here, P_{out}, PAE, and gain are considered as averages in the operating band. According to FOM values, this work has the best FOM value compared to other similar studies.

IV. CONCLUSIONS

This article presents a systematic set of steps of 25 W PA design. A deep AB class high-power and high-efficiency PA has been designed and manufactured for use in radar and wireless

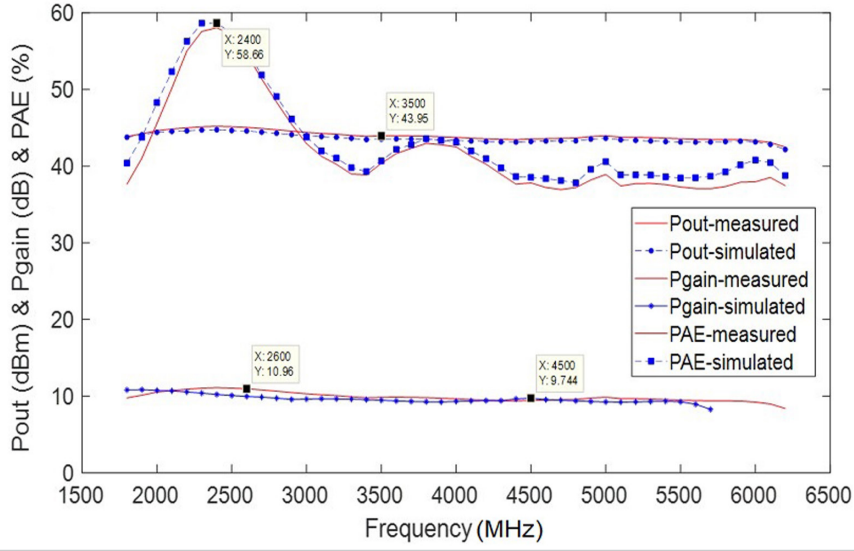

Fig. 16. Output power and PAE curves according to frequency (P_{in} = 34 dBm).

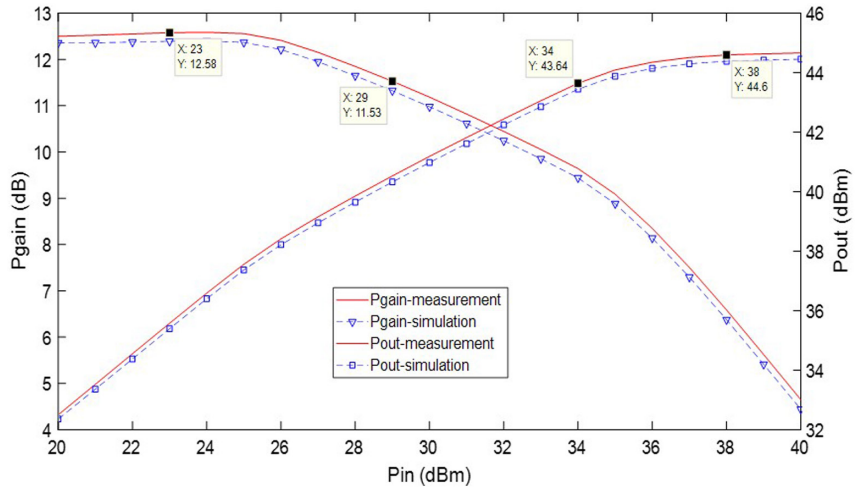

Fig. 17. Output power versus input power.

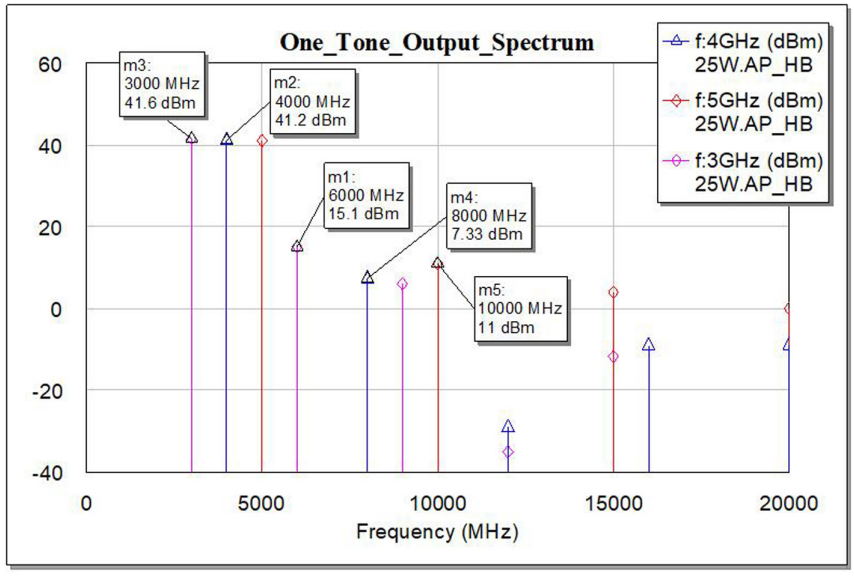

Fig. 18. The one tone output spectrum of the 25W PA.

communication systems. In the study, a rigorous analysis has been carried out on the DC and RF electrical characteristics of the transistors. A detailed SP and LP analyses have been performed to design IMN and OMN. The experimental results show that a P_{out} of 43.8 dBm, 9.8 dB gain, PAE of 41–57%, and second harmonic level lower than –26 dBc are achieved across the 2–6 GHz operation band.

TABLE I. COMPARISON TABLE ON THE PERFORMANCE OF POWER AMPLIFIERS IN THE LITERATURE.

Ref.	BW (GHz)	P_{out} (dBm)	PAE (%)	Gain (dB)	FOM (1K)*
[12]	2–6	43.5–44	40–50	8–9	5.738
[13]	1.7–3	44	65	10.7	2.869
[14]	1.7–2.8	44	58–66	10	2.122
[15]	3.95–4.35	44	57–67	12	0.78
This work	2–6	~43.8	41-57	~9.8	6.46

Availability of Data and Materials: The data that support the findings of this study are available on request from the corresponding author.

Peer-review: Externally peer-reviewed.

Author Contributions: Concept – E.Ç.; Design – E.Ç.; Supervision – O.K., M.Y.; Materials – O.K.; Data Collection and/or Processing – E.Ç.; Analysis and/or Interpretation – E.Ç., O.K., M.Y.; Literature Search – E.Ç.; Writing – E.Ç.; Critical Review – O.K., M.Y.

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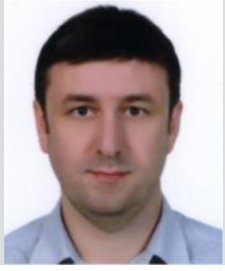

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