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Improved Interleaved Buck Converter with High-Step Down Conversion Ratio and Soft-Switching

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ABSTRACT

This article proposes a new interleaved buck converter with a high step-down conversion ratio and soft-switching. The soft-switching conditions for the main IGBTs are achieved with the aid of a simple auxiliary circuit, which comprises a resonant inductor, a resonant capacitor, and a diode. A new interleaved buck converter is realized by adopting two auxiliary circuits separately connected to each one of the legs to provide zero voltage switching (ZVS) and zero current switching (ZCS) turn-on operation. The major advantages of this converter are reduced switching losses, a high step-down ratio, reduced voltage stresses, and no limitation on duty ratio. To validate the theoretical analysis, a laboratory prototype of a 200 V–60 V converter system has been developed and achieved an efficiency of 96% at 250 W output power.

***Index Terms*—**High step-down, interleaved buck converter, soft-switching, zero voltage switching (ZVS)

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I. INTRODUCTION

Buck converters find widespread application in scenarios requiring low output voltage and high output current, such as battery chargers, voltage regulator modules (VRMs) in the central processing units (CPUs) of computer systems, uninterruptible power supplies (UPSs), electric vehicles (EVs), and hybrid EVs [1-3]. In early days, a two-phase interleaved buck converter (TIBC) [4] incorporating a passive clamp circuit and coupled inductor was utilized. This implementation offered benefits such as reduced output current ripples, minimized voltage spikes, and an enhanced step-down ratio. Subsequently, improvements were made to TIBCs [5] by integrating a voltage-divider network and employing additional blocking capacitors to alleviate voltage stress on the main switching devices, thereby mitigating extreme short-duty cycles and achieving the desired voltage conversion ratio. Nevertheless, these enhancements also led to an increase in the number of switching devices and necessitated the incorporation of additional capacitors.

To increase overall efficiency, a buck converter with reduced output ripples and achieving soft-switching characteristics such as ZVS and zero current switching (ZCS) are the best solutions. In a Single Switch Buck Converter (SSBC) [6], ZVS turn-on operation to the main switch is achieved by utilizing the leakage inductance of a coupled inductor, an auxiliary switch, and a snubber capacitor. In addition to a coupled inductor in SSBC [7], an auxiliary passive circuit is used to achieve ZCS turn-on and ZVS turn-off characteristics. Similarly, ZCS turn-on and turn-off conditions are realized in another SSBC [8], which utilized the coupled inductor technique with three leakage inductances considered in addition to resonant elements.

Furthermore, the zero current transition (ZCT) condition is realized in a non-coupled inductor-based two-switch buck converter (TSBC) [9] by adopting an output inductor. In a two-channel buck converter (TCBC) [10] used for driving LEDs, a single series capacitor can be employed to balance the current across all channels, potentially simplifying the design by eliminating the need for separate control circuitry. However, this approach may be limited to applications with very low output power levels. To minimize the output ripples in a two-phase buck converter [11],

series connections of coupled inductors provide a viable solution, and in addition to that, a lossless snubber is included to obtain the ZCS turn-on condition. In a TSBC [12, 13], additional input inductors and switched-capacitor cells are utilized to obtain the desired high step-down ratio. To develop ripple-free high-power applications, interleaved buck converters [14-16] are preferable with a simple series capacitor in addition to a coupled inductor, and those converters are further improved with a valley-fill capacitor cell (VFCC) [17] by replacing series capacitors to ensure desired conversion ratios.

In this paper, a novel interleaved buck converter is realized with soft switching and a high step-down conversion ratio. To ensure soft switching operation of the main switches, two auxiliary circuits are adopted to a conventional buck converter. To provide the desired conversion ratio, a series capacitor is used in the power flow path. The proposed converter offers the following advantages:

- No auxiliary switches are used.
- ZVS turn-on for the main switch S_1.
- ZCS turn-on for the main switch S_2.
- Fewer additional devices.
- The voltage across switching devices is less than the input voltage.

II. DESCRIPTION AND OPERATING MODES

A. Description of Proposed Interleaved Buck Converter

An improved soft-switching interleaved buck converter, shown in Fig. 1, consists of two main switching devices (S_1, S_2) connected in series, a coupling capacitor (C_s) is placed in the power flow path, and two output inductors (L_1, L_2). In order to provide zero voltage switching (ZVS) turn-on condition to switch S_1, and zero current switching (ZCS) turn-on condition to switch S_2, the resonant network L_m, C_m, and D_m is connected to the leg of switch S_1, and another resonant network L_n, C_n, and D_n is connected to the leg of S_2.

The major merits of this topology are:

- Voltage stresses of the main IGBTs are half of the input voltage.
- Reduced switching losses.
- Lower output current ripple.
- Lower conversion ratio.
- Soft-switching conditions: ZVS and ZCS.

Fig. 2 shows the PWM signals V_{G1} and V_{G2} for switches S_1, and S_2 respectively, with duty cycle (D) intervals t_2–t_3 and t_6–t_7, representing the controlled switching actions in the interleaved buck converter. A minimal duty ratio (D) of 20% has been chosen for both S_1 and S_2 to ensure the desired conversion ratio. The operation of this converter is divided into seven modes, denoted as t_0–t_7, as illustrated by the key waveforms in Fig. 2 and corresponding equivalent circuits for all the modes are shown in Figs. 3-9.

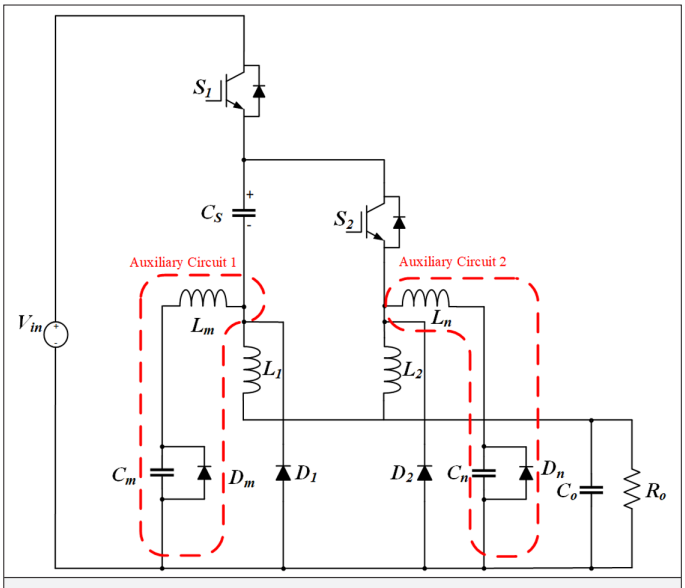

Fig. 1. Proposed schematic of interleaved buck converter with high step-down conversion ratio

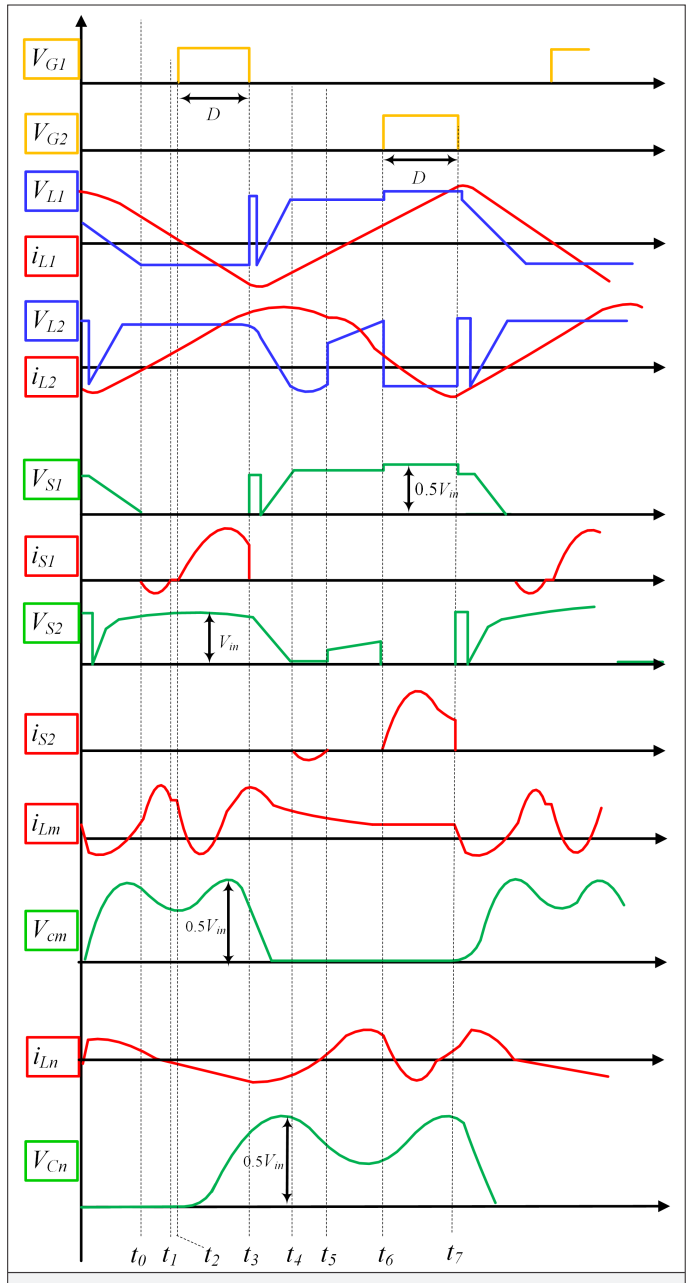

Fig. 2. Key waveforms. (Note that the waveforms are represented from the obtained simulation results.)

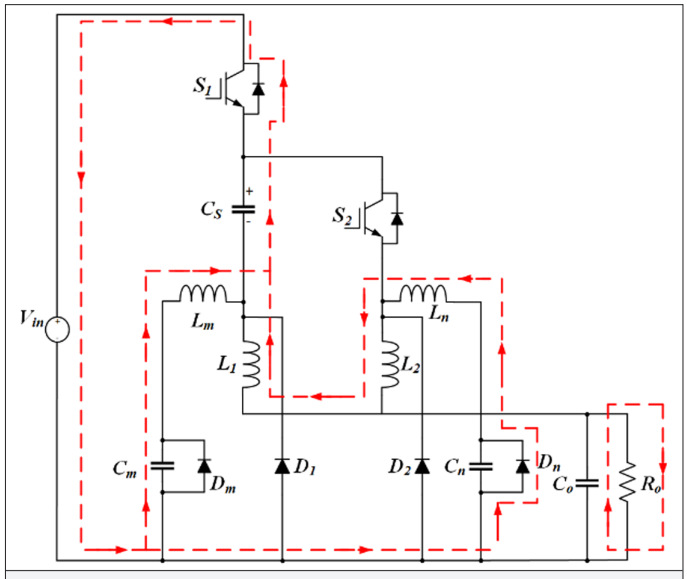

Fig. 3. Equivalent circuit: mode 1 (t_0–t_1).

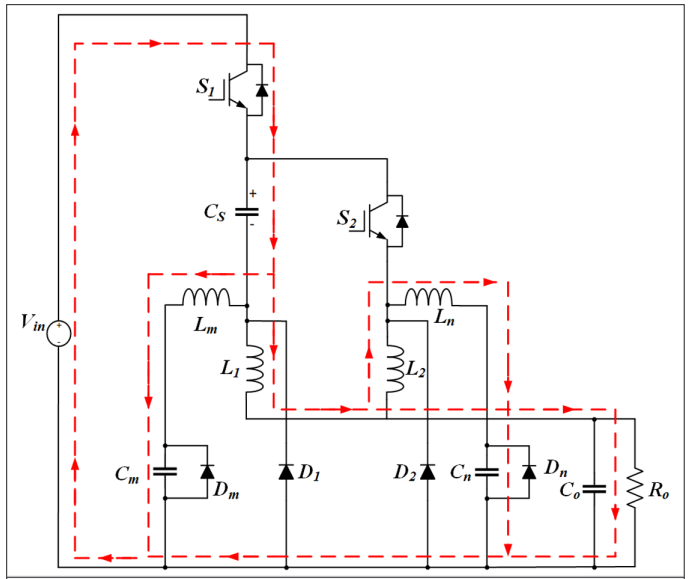

Fig. 5. Equivalent circuit: mode 3 (t_2–t_3).

B. Operating Modes

Mode 1 (t_0–t_1): At t_0, body diode of IGBT, S_1 is begins conducting to provide the path of resonant tank current. Therefore, it fulfills the ZVS turn-on condition. At the end of this interval, the S_1 body diode stops conducting. The governing equations of i_{S1}, V_{Cm}, i_{L1}, and i_{Ln} are expressed in:

$$i_{S1}(t) = 0 \tag{1}$$

$$V_{Cm}(t) = V_{Cm}(t_0) + V_{Cm}(t_0)(1 - \cos\omega_1(t - t_0)) \tag{2}$$

where $\omega_1 = \dfrac{1}{\sqrt{(L_n + L_2 + L_1 + L_m)\left(\dfrac{C_m \times C_n}{C_m + C_n}\right)}}$

$$i_{Ln}(t) = i_{Ln}(t_0) + \left(V_{Cn}(t_0) - V_0\right)\sqrt{\frac{C_n}{L_n + L_2}} \times \sin\omega_2(t - t_0) \tag{3}$$

where $\omega_2 = \dfrac{1}{\sqrt{(L_n + L_2)C_n}}$

$$i_m(t) = i_{Ln}(t) - I_0 \tag{4}$$

$$V_{Cn}(t) = V_n(t_0)\cos\omega_2(t - t_0) \tag{5}$$

Mode 2 (t_1–t_2): During this mode, IGBT, S_1 current reaches zero and C_m discharges to V_{in}.

Mode 3 (t_2–t_3): At t_2, S_1 is turned on with zero voltage and zero current switching (ZVZCS) condition. Throughout this mode, the output power flows via V_{in}–S_1–L_1. The governing equations for i_{Lm}, i_{L1}, i_{L2}, V_{Cm}, and V_{Cn}.

$$i_{S1}(t) = V_{in}\sqrt{\frac{C_{eq}}{L_m}}\,\mathrm{Sin}\omega_3(t - t_2) \tag{6}$$

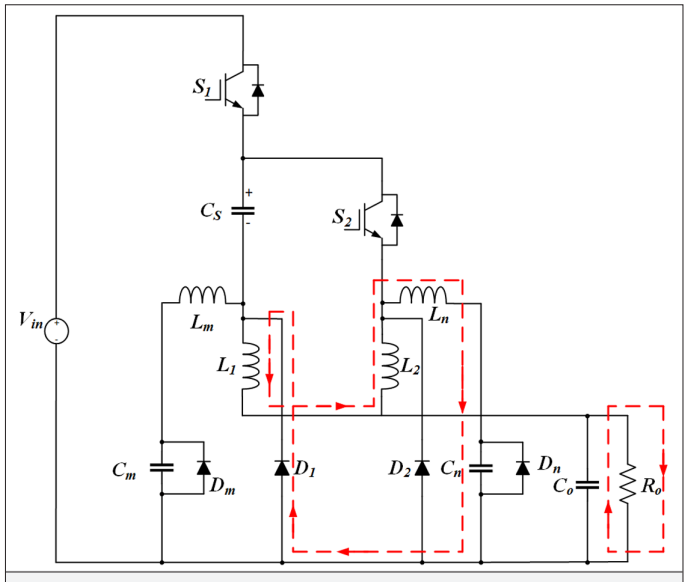

Fig. 4. Equivalent circuit: mode 2 (t_1–t_2).

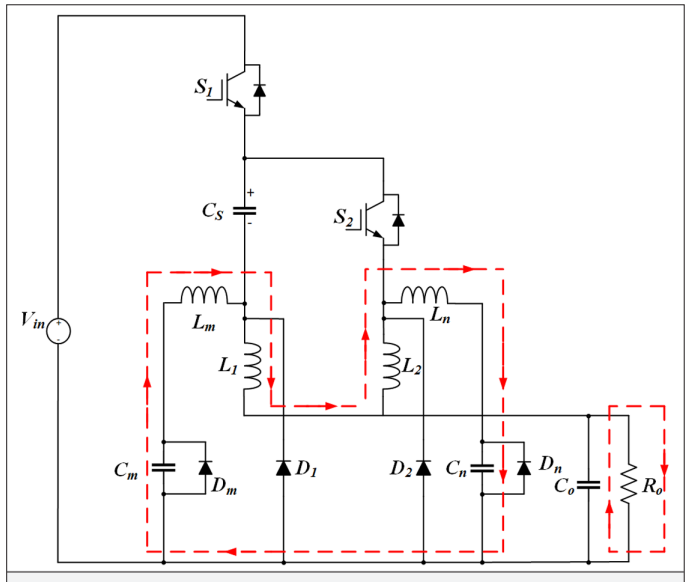

Fig. 6. Equivalent circuit: mode 4 (t_3–t_4).

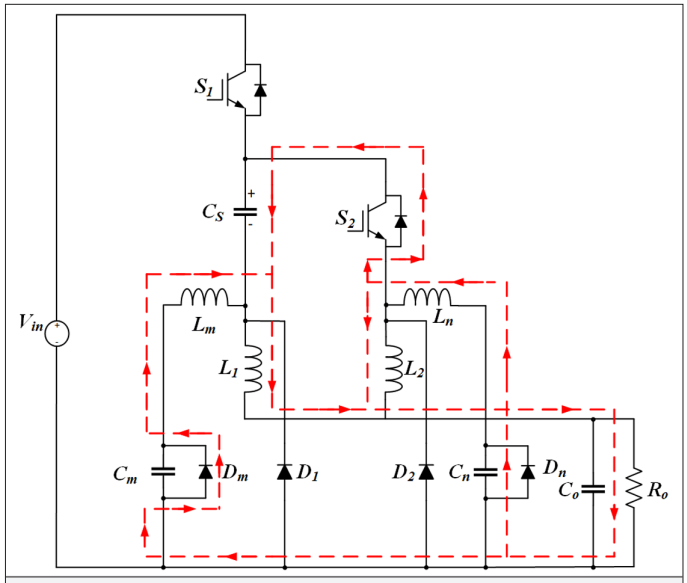

Fig. 7. Equivalent circuit: mode 5 (t_4–t_5).

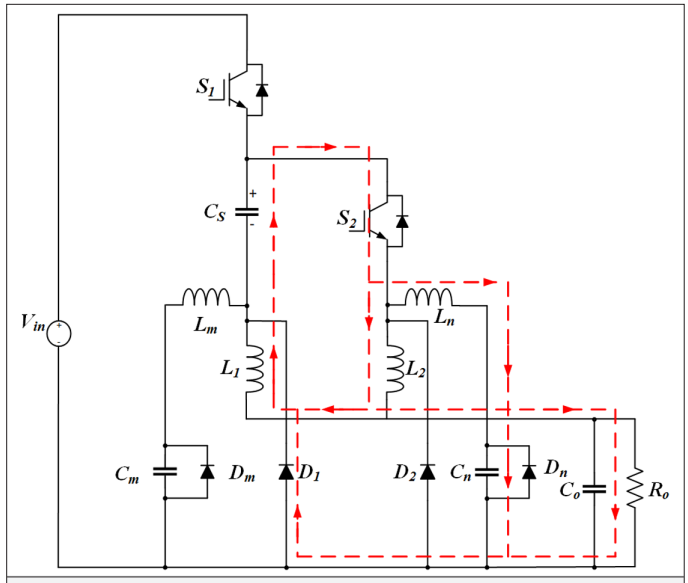

Fig. 9. Equivalent circuit: mode 7(t_6–t_7).

where $C_{eq} = \frac{C_S \times C_m}{C_S + C_m}$ and $\omega_3 = \frac{1}{\sqrt{L_m C_{eq}}}$

$$V_{cm}(t) = V_{cm}(t_2) + V_{cm}(t_2)\left[1 - \cos\omega_4(t - t_2)\right] \quad (7)$$

where $\omega_4 = \frac{1}{\sqrt{L_m C_m}}$

$$i_{L1}(t) = i_L(t_2) + \frac{1}{L_1}[V_{in} - V_{Cs} - V_o](t - t_2) \quad (8)$$

$$i_{Ln}(t) = i_{L1}(t_2) - I_0 \sin\omega_5(t - t_2) \quad (9)$$

where $\omega_5 = \frac{1}{\sqrt{L_{eq} C_n}}$ and $L_{eq} = L_1 + L_2 + L_n$

Mode 4 (t_3–t_4): During this mode, the voltage across IGBT S_1 linearly increases and S_2 falls to zero at the end of this interval. C_n is charged to 0.5V_{in} at t_4 and C_m is completely discharged to zero. The expressions for i_{Lm}, i_{L1}, i_{L2}, V_{Cm}, and V_{Cn} are as follows:

$$i_{S2}(t) = \left(V_{Cs}\sqrt{\frac{C_{eq1}}{L_n}}\right)\sin\omega_6(t - t_3) \quad (10)$$

where $\omega_6 = \frac{1}{\sqrt{L_n C_{eq1}}}$; $C_{eq1} = \frac{C_S \times C_n}{C_S + C_n}$

$$V_{cn}(t) = V_n(t_3) + i_{S2}(t)\sqrt{\frac{L_n}{C_{eq1}}}\sin\omega_6(t - t_3) \quad (11)$$

$$i_{L2}(t) = i_{L2}(t_3) + V_{Cs}\sqrt{\frac{C_s}{L_2 + L_1}}\sin\omega_7(t - t_3) \quad (12)$$

where $\omega_7 = \frac{1}{\sqrt{(L_2 + L_1)C_s}}$

Mode 5 (t_4–t_5): Throughout this mode, the body diode of S_2 is in a conducting state and L_n, C_n are in a resonating state. The governing equations for i_{Lm}, i_{L1}, i_{L2}, V_{Cm}, and V_{Cn} are expressed in:

$$i_{S1}(t) = 0 \quad (13)$$

$$i_{Lm}(t) = i_{Lm}(t_4) + \left(\frac{V_o}{L_1 + L_m}\right)(t - t_4) \quad (14)$$

$$i_{L2}(t) = \left(\frac{V_{Cn}(t_4) - V_o}{L_n + L_2}\right)(t - t_4) \quad (15)$$

where $\omega_8 = \frac{1}{\sqrt{(L_n + L_1)C_s}}$

$$i_{S1}(t) = \left(V_{Cn}(t_4) - V_{Cs} - V_o\right)\sqrt{\frac{C_s}{L_n + L_1}}\sin\omega_8(t - t_4) \quad (16)$$

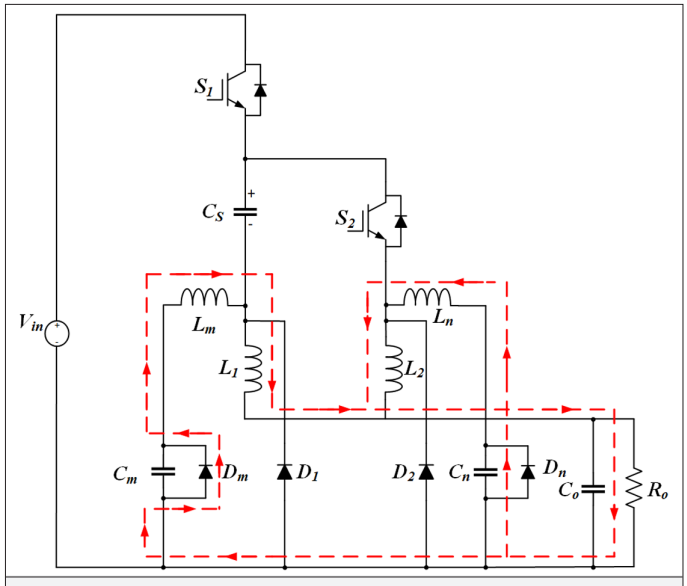

Fig. 8. Equivalent circuit: mode 6 (t_5–t_6).

Mode 6 (t_5–t_6): During this mode, the voltage across IGBT, S_2 reaches V_o and still L_n, C_n are in a resonating condition. The corresponding equations for $i_{S1,}$ i_{Ln}, i_{L1}, i_{L2}, V_{Cm}, and V_{Cn} are expressed as follows:

$$i_{S1}(t)=0 \tag{17}$$

$$V_{Cm}(t)=0 \tag{18}$$

$$i_{Lm}(t)=i_{Lm}(t_5) \tag{19}$$

$$V_{cn}(t)=V_{in}(t_5)+i_{s2}(t)\sqrt{\frac{L_n}{C_{eq1}}}\sin\omega_6(t-t_5) \tag{20}$$

$$i_{Ln}(t)=i_{S2}(t)-i_{L2}(t) \tag{21}$$

Mode 7 (t_6–t_7): At $t_{6,}$ IGBT S_2 is turned on with zero current switching (ZCS), and output power flows via V_{in}–S_2–L_2.

$$i_{S2}(t)=V_{Cs}\sqrt{\frac{C_{eq1}}{L_n}}\sin\omega_6(t-t_6) \tag{22}$$

$$V_{cn}(t)=V_{in}(t_6)+i_{s2}(t)\sqrt{\frac{L_n}{C_{eq1}}}\sin\omega_6(t-t_6) \tag{23}$$

$$i_{Lm}(t)=i_{S2}(t)-i_{L2}(t) \tag{24}$$

$$i_{L2}(t)=i_{L2}(t_6)+V_{Cs}\sqrt{\frac{C_s}{L_2+L_1}}\sin\omega_9(t-t_6) \tag{25}$$

where $\omega_9=\dfrac{1}{\sqrt{(L_1+L_2)C_s}}$

III. DC CONVERSION RATIO

The conversion ratio of this converter is determined through the utilization of the voltage–second balance (V-S-B) equation on L_1 and L_2. Typically, the conversion ratio is calculated by examining two operational conditions: the first condition when IGBT S_1 is ON state and the second condition when the IGBT, S_1 is in the OFF state.

Apply V-S-conB on $L_{1,}$ when S_1 is turned-on, L_1 voltage can be written as:

$$V_{L1}=V_{in}-V_{Cs}-V_0 \tag{26}$$

When S is turned off, then L_1 voltage can be expressed as:

$$V_{L1}=-V_0 \tag{27}$$

Apply V-S-B on $L_{1,}$ when S_2 is turned-on, L_1 voltage can be written as:

$$V_{L2}=V_{Cs}-V_0 \tag{28}$$

When S_2 is turned off, then L_1 voltage can be expressed as:

$$V_{L2}=-V_0 \tag{29}$$

Applying Volt–second balance for the inductor, L_1,

$$\left(V_{in}-V_{Cs}-V_0\right)D+(-V_0)(1-D)=0 \tag{30}$$

$$\left(V_{in}-V_{Cs}\right)D=V_0D+(V_0)(1-D) \tag{31}$$

$$\left(V_{in}-V_{Cs}\right)D=V_0 \tag{32}$$

Applying Volt–second balance for the inductor, L_2,

$$\left(V_{Cs}-V_0\right)D+(-V_0)(1-D)=0 \tag{33}$$

$$V_{Cs}D=V_0 \tag{34}$$

$$V_{Cs}=\frac{V_0}{D} \tag{35}$$

The voltage of the coupling capacitor C_S can be obtained by (28) and (29), which equals to half of the input voltage. The voltage conversion ratio of the converter is given by:

$$\left(V_{in}-\frac{V_0}{D}\right)D=V_0 \tag{36}$$

$$V_{in}D=2V_0 \tag{37}$$

$$\frac{V_0}{V_{in}}=\frac{D}{2} \tag{38}$$

IV. DESIGN ANALYSIS

The criteria for achieving soft-switching conditions ZVS/ZCS during the turn-on of the switches S_1 and S_2 are established through the inequality defined in (39). Increasing the value of characteristic impedance (Z) helps in reducing the peak currents across the switching devices. Maintaining the parameter I_z at minimal levels is necessary to ensure the ZVS and ZCS turn-on conditions.

$$I_Z\geq I_o \tag{39}$$

$$I_Z=\frac{V_{in}}{\sqrt{\frac{L_{m,n}}{C_{m,n}}}} \tag{40}$$

The resonant inductors L_m, L_n and capacitors, C_m, C_n are constrained by the resonant frequency:

$$f_r=\frac{\omega}{2\pi}=\frac{1}{2\pi\sqrt{L_{m,n}C_{m,n}}} \tag{41}$$

The following variables are defined:

Characteristic impedance,

$$Z=\sqrt{\frac{L_{m\approx n}}{C_{m\approx n}}} \tag{42}$$

Resonant angular frequency,

$$\omega=\frac{1}{\sqrt{L_{m\approx n}C_{m\approx n}}} \tag{43}$$

Resonant capacitors C_m, C_n are selected by the following relation:

$$C_{m\approx n}\leq\frac{1}{\omega}\left(\frac{I_o}{V_{in}}\right)\left(\frac{1}{2f_s}\right) \tag{44}$$

Resonant inductors L_m, L_n are selected by the following relation:

$$L_{m\approx n} = \frac{1}{C_{m\approx n}(2\pi f_r)^2} \tag{45}$$

Normalized frequency is defined by,

$$f_n = \frac{f_r}{f_s} \tag{46}$$

The selection of switches S_1, S_2 depends on peak voltage stress and current stresses:

$$V_{S1} = \frac{V_{in}}{2} \tag{47}$$

$$V_{S2} = V_{in} \tag{48}$$

$$I_{S1,S2} = I_z + I_o \tag{49}$$

The selection of diodes D_m, D_n depends on current stress:

$$I_{Dm\approx n} = I_o \tag{50}$$

The voltages across the capacitor C_m, C_n are defined by:

$$V_{Cm\approx n} = 2V_{in} \tag{51}$$

The selection of IGBTs and diodes in the converter is made based on (47), (48), and (49). The maximum current stresses of the IGBTs and diodes are 10A, and voltage across the IGBT is equals to the input voltage. The maximum value of resonant capacitors C_m, C_n can be used below 40 nF, and resonant inductors can be selected at 30 μH from (44) and (45), respectively.

V. LOSS DISTRIBUTION OF THE PROPOSED CONVERTER

This section presents the loss distribution of the proposed converter while operating at 250 W output power with 200 V input voltage and 60 V output voltage; output current: 4.16 A.

A. Switch Losses

The RMS current of the switch is calculated by:

$$i_{sw(rms)} = I_o + V_{cm} \times \sqrt{\frac{C_m}{L_m}} \tag{52}$$

Power loss in the switch

$$P_{sw} = i_{sw(rms)}{}^2 \times r_{(on)} + \frac{V_{sw} \times i_{sw} \times f_{sw}(t_r + t_f)}{6} \tag{53}$$

where $r_{L\ =}$ on-state resistance

B. Inductor Losses

The RMS current in the inductor ($i_{L1(rms)}$) is calculated by:

$$i_{L1(rms)} = I_o \sqrt{D\left(1 + \frac{\Delta i_L}{i_{L\min}}\left(1 + \frac{1}{3} \times \frac{\Delta i_L}{i_{L\min}}\right)\right)} \tag{54}$$

where Δi_L = input ripple; i_{Lmin}=minimum input current; I_o=output current

Power loss of the inductors

$$P_{Lloss(rms)} = I_{L(rms)}{}^2 \times r_L \tag{55}$$

where r_L = inductor internal resistance

C. Diode Losses

The diodes D_1, D_2 rms average currents ($I_{D1(rms)}$,$I_{D1(avg)}$) and total power loss ($P_{loss(rms)}$) are given by

$$I_{D1(rms)} = \frac{V_{cs} - V_o}{2\pi} \sqrt{\frac{C_s}{L_2}} \sqrt{\frac{D}{3}} \tag{56}$$

where $V_{cs} = \frac{V_{in}}{2}$

$$I_{D1(avg)} = \frac{V_{cs} - V_o}{2\pi} \times \sqrt{\frac{C_s}{L_2}} \times D \tag{57}$$

$$P_{loss(rms)} = I_{d(rms)}{}^2 \times r_d + V_\gamma \times i_{d(avg)} \tag{58}$$

where $V\gamma$ = forward voltage drop.

The diodes D_m, D_n rms and average currents ($I_{Dm(rms)}$,$I_{Dm(avg)}$) are given by**:**

$$I_{Dm(avg)} = \frac{V_{cs} - V_o}{2\pi} \sqrt{\frac{C_S}{L_m + L_2}} \times D \tag{59}$$

$$I_{Dm(rms)} = \frac{V_{cs} - V_o}{2\pi} \sqrt{\frac{C_S}{L_m + L_2}} \times \sqrt{\frac{D}{3}} \tag{60}$$

$$P_{Dloss} = I_{d(rms)}{}^2 \times r_d + V_\gamma \times I_{d(avg)} \tag{61}$$

It can be seen from Table I, by using equations (52–61), that the losses in the diodes are 4.28 W, the losses in inductors are 2.88 W, and the losses

TABLE I. OVERALL LOSSES OF THE PROPOSED CONVERTER

Device Type	Components	$r_{(on)}$ ($m\Omega$)	V_{max} (V)	$V\gamma$ (V)	I_{avg} (A)	I_{max} (A)	Loss (W)	Loss Percentage
Diode	D_m, D_n, D_1, D_2	2	250	0.8	1.9	6.3	4.28	44.31
Switch	S_1, S_2	33	240	–	4.6	7.8	2.02	20.91
Inductor	L_a, L_b, L_m, L_n	60	–	–	0.81	2.29	2.88	29.81
Capacitor	C_a, C_b, C_o	1000	250	–	–	0.14, 0.14, 1.01	0.484	4.97
Total losses in the converter							9.664	100.00

in capacitors are 0.484 W. The switching losses are reduced as soft-switching is implemented to turn on the switches, which is 2.02 W. The overall losses are 9.664 W, while the converter operates at 250 W output power, obtaining an overall efficiency of the converter of 96.13%. The loss distribution of the proposed converter is shown in Fig. 10.

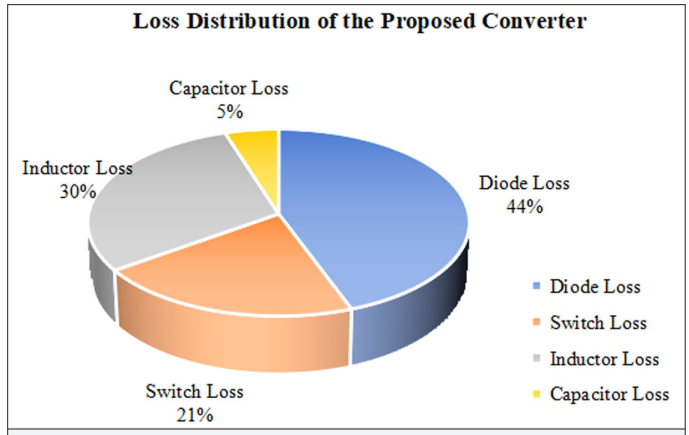

Fig. 10. Loss distribution of the proposed converter.

VI. SIMULATION RESULTS

The converter is designed using the PLECS simulation tool. The proposed converter is simulated with the following parameters:

- Input voltage: 200 V
- Output voltage: 60 V
- Output resistance: 50 Ω
- Switching frequency: 40 kHz
- Output power: 250 W

Fig. 11 shows the voltage and current waveforms of the main IGBTs S_1 and S_2. It can be seen from the obtained results that the voltage stress of S_1 is equal to half of the input voltage, and S_2 is also less than the input voltage. The resonant networks are employed for both legs separately. These help in providing ZVZCS and ZCS condition turn-on for S_1 and S_2 switching devices, respectively.

Fig. 12 shows the voltages of C_m, C_n, and current waveforms L_m, L_n. Current through the inductor equals the output current, and voltage across C_m, C_n is 160 V, each. Fig. 13 depicts the current waveforms of the output inductors L_1 and L_2.

VII. EXPERIMENTAL RESULTS

To validate the theoretical analysis, a laboratory prototype of the proposed 200V-60V-250W converter system was implemented. The experimental setup's parameters and components are detailed in Table II. Experimental verifications were performed under open-loop conditions, and PWM signals were generated using a TMSF28335 docking station. Two SKYPER 32R drivers were used to generate the desired 40 kHz switching frequency. Ferrite E-cores were utilized for inductors, L_1 and L_2, each with 100 µH, along with resonant inductors L_m and L_n, and each with 30 µH. Polypropylene (PP) film capacitors,

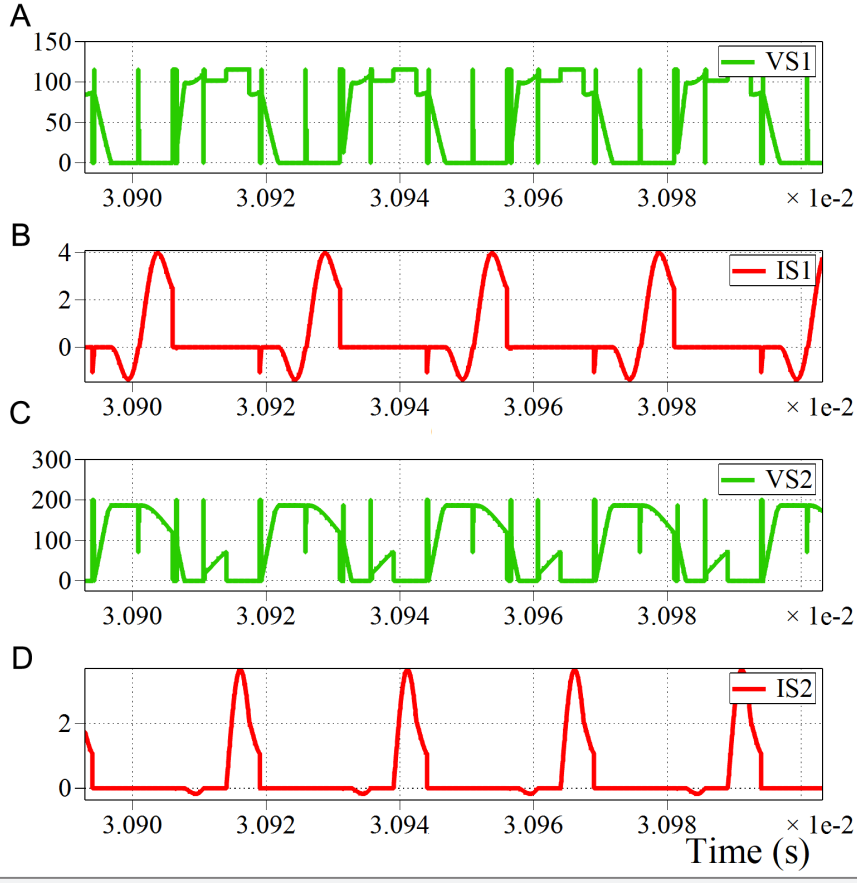

Fig. 11. PLECS simulation waveforms: (a) $V_{S1,}$ (b) $i_{S1,}$ (c) *V*S2, and (d) i_{S2}.

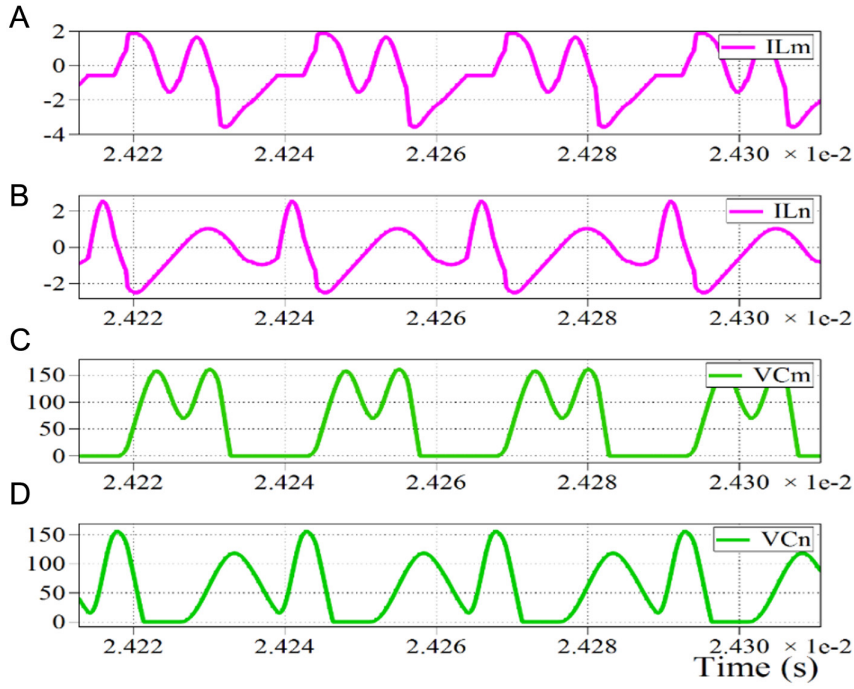

Fig. 12. PLECS simulation waveforms: (a) $i_{Lm,}$ (b) $i_{Ln,}$ (c) $V_{Cm, and}$ (d) V_{Cn}.

specifically WIMA FKP1R013304C, were employed for resonant capacitors C_m and C_n, with a total capacitance of 40 nF achieved by connecting 12 numbers of 3300 pF capacitors in parallel. WOLFSPEED SiC SCHOTTKY diodes C6D06065A were used as D_m and D_n, while Infineon IGBTs IHW25N120R2 served as S_1 and S_2. The PWM signals had a 20% duty cycle during measurements. The converter was tested with a 200 V input voltage, yielding a 60 V output voltage with a 20% duty cycle and a load resistance (R_0) of 40 Ω. Waveforms of the main switching devices S_1 and S_2 are presented in Fig. 14, indicating a voltage of 100 V across S_1 and 200 V across S_2, with peak currents of 7A and 5A, respectively. Both switches exhibited zero voltage and zero current turn-on conditions without additional losses. Fig. 15 shows waveforms of L_m and L_n, with an average current of 5A.

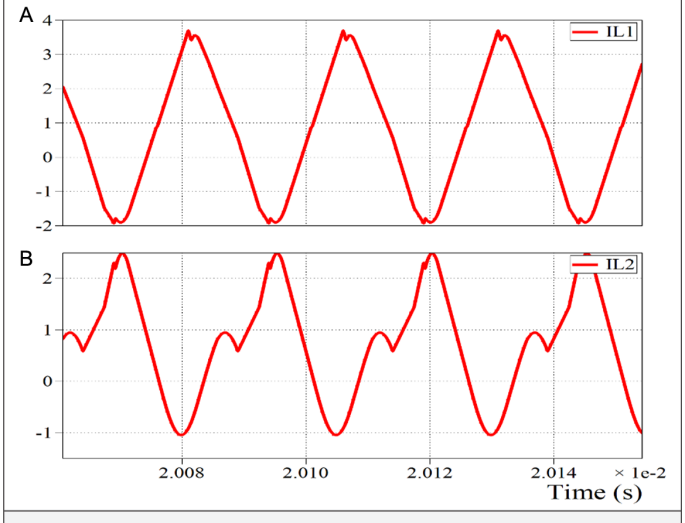

Fig. 13. PLECS simulation waveforms: (a) $i_{L1 and}$ (b) i_{L2}.

Fig. 16 illustrates the voltage across resonant capacitors C_m and C_n, showing a maximum voltage of approximately 200 V for each capacitor. Figs. 17 and 18 depict the current through inductors L_1, L_2, and diodes D_m, D_n, respectively, with peak currents matching the output current. Fig. 19 shows the turn-on and turn-off transitions of S_1 and S_2 at a maximum output power of 250 W. Fig. 20 shows a plotted curve between efficiency versus output power. It can be seen that the lower efficiency obtained at 150 W output power is 93%, and at 250 W output power, 96.2% is the maximum efficiency. Voltage conversion ratios are plotted in Fig. 21 between two topologies: one is conventional interleaved buck converter and the other one is extended interleaved buck converter. Fig. 22 shows the hardware prototype developed for the proposed interleaved buck DC-DC converter. Table III illustrates the comparison of existing topologies with the proposed converter. A higher number of auxiliary switches are

TABLE II. PROTOTYPE PARAMETERS

Parameter	Symbol	Value
Input voltage	V_{in}	200 V
Output power	P_o	250 W
Switching frequency	f_{sw}	40 kHz
Resonant inductors	L_m, L_n	30 µH
Resonant capacitors	C_m, C_n	40 nF
Inductors	L_1, L_2	100 µH
Output capacitor	C_o	470 µF
IGBTs	S_1, S_2	IHW25N120
Diodes	D_1, D_2, D_m, D_n	C6D06065A

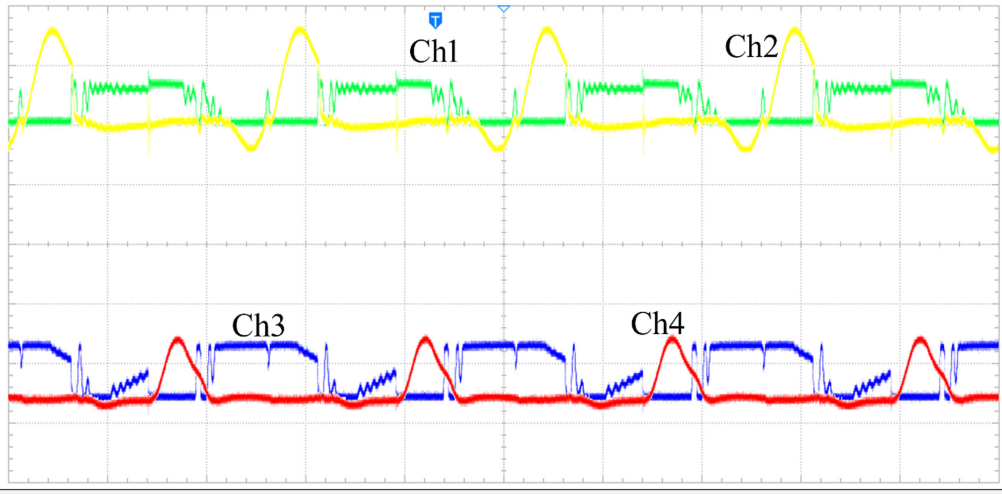

Fig. 14. Measured waveforms of V_{S1}, V_{S2}, i_{S1}, i_{S2} collector-emitter voltage $V_{S1,}$ Ch1: 250V/div (Top); collector current $i_{S1,}$ Ch2: 5A/div (Top). Collector-emitter voltage $V_{S2,}$ Ch3: 250V/div (Bottom). Collector current $i_{S2,}$ Ch4: 5A/div (Bottom). Time scale: 10 µs/div.

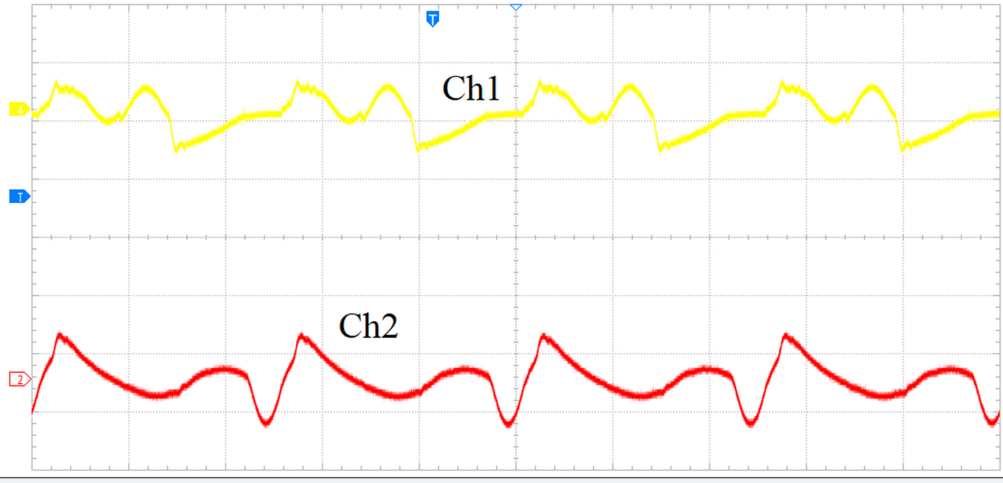

Fig. 15. Measured waveforms of current through L_m and L_n Current through L_m Ch1: 5A/div (Top); Current through L_n Ch2: 5A/div (Bottom). Time scale: 10 µs/div.

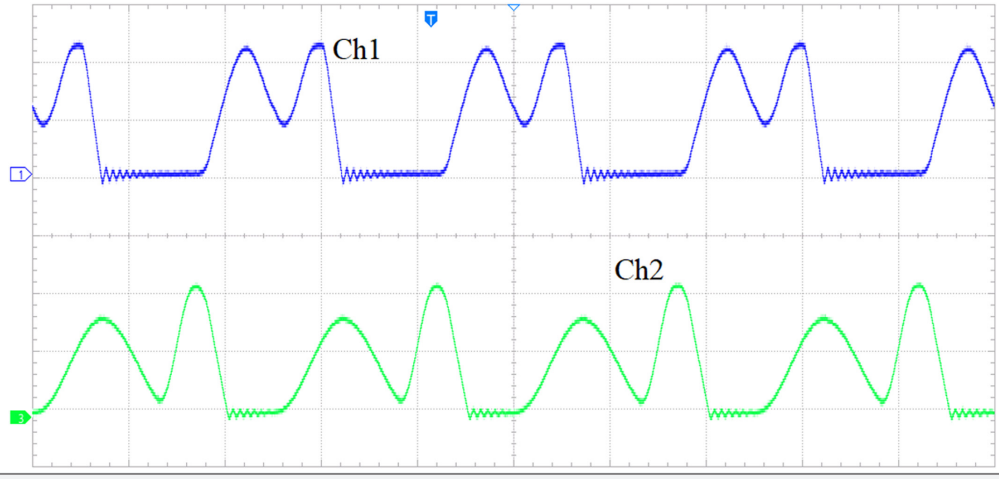

Fig. 16. Measured waveforms of V_{Cm} and V_{Cn} Voltage across C_m Ch1: 100V/div (Top); Voltage across C_n Ch2: 100V/div (Bottom). Time scale: 10 µs/Div.

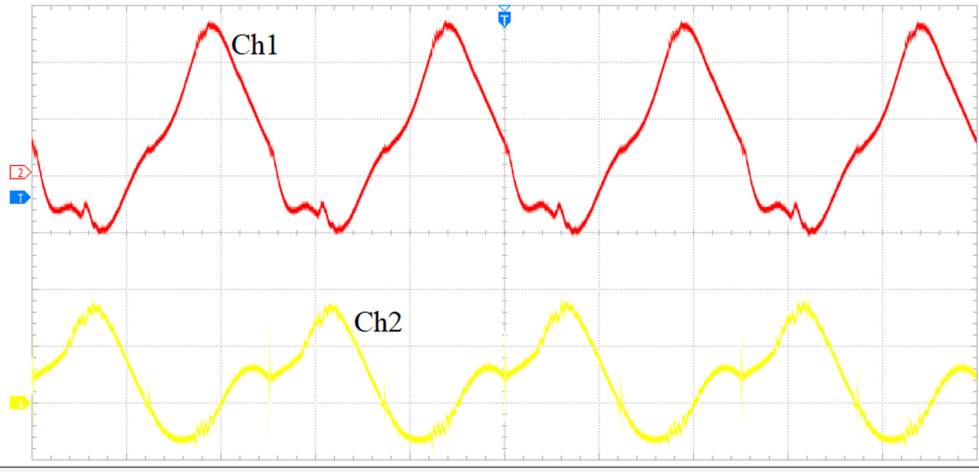

Fig. 17. Measured waveforms of current through L_1 and L_2 current through L_1 Ch1: 2A/div (Top); current through L_2 Ch2: 2A/div (Bottom). Time scale: 10 µs/div.

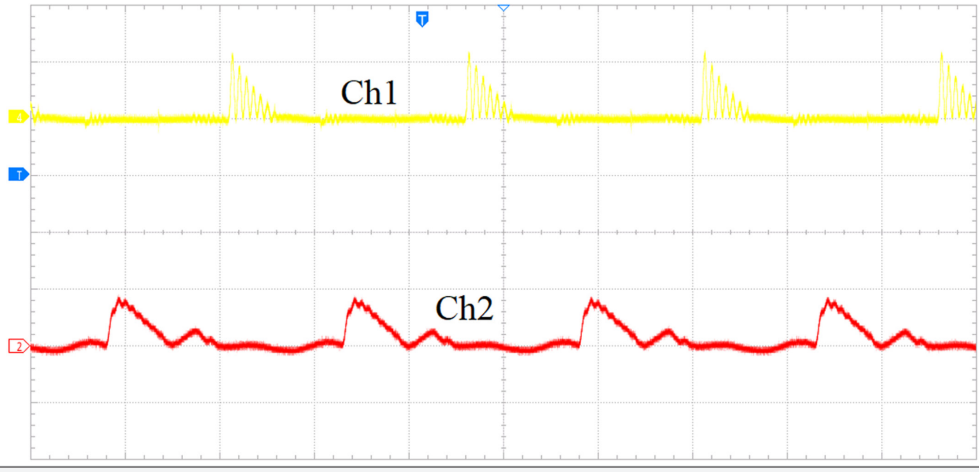

Fig. 18. Measured waveforms currents through diodes D_m and D_n. Currents through diodes D_m Ch1: 5A/div (Top); Current through diode D_n Ch2: 5A/div (Bottom). Time scale: 5 µs/div.

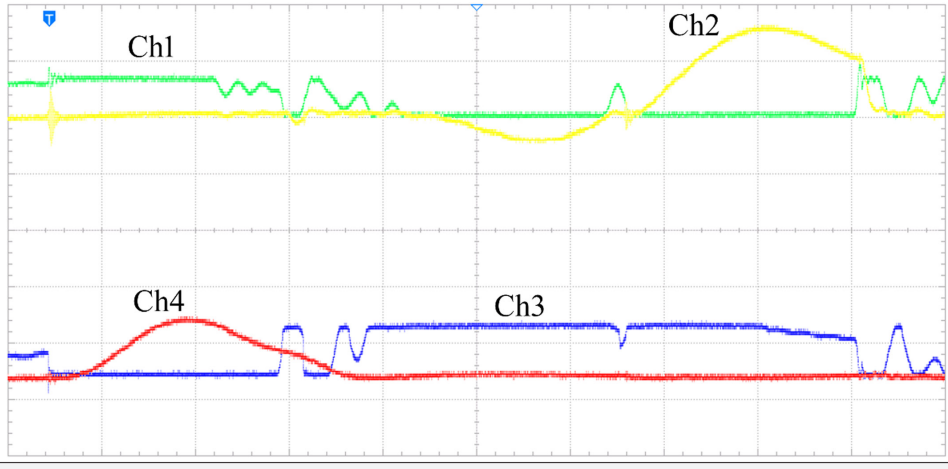

Fig. 19. Measured waveforms of $V_{S1,}$ $i_{S1,}$ $V_{S2,}$ i_{S2} collector-emitter voltage V_{S1} (Ch1: 100V/div); collector current i_{S1} (Ch2: 5A/div) (Top); collector-emitter voltage $V_{S2,}$ (Ch1: 100V/div); collector current i_{S2} (Ch2: 5A/div) (Bottom). Time scale: 4 µs/Div.

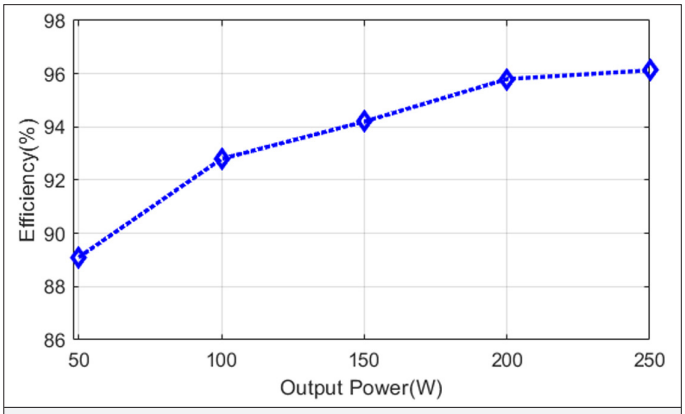

Fig. 20. Efficiency curve.

used in the existing topologies [5, 6, 11-13] than in the proposed topology. The proposed converter has much better efficiency with a fewer number of auxiliary devices, and voltage and current stresses are lesser than the existing topologies. The overall efficiency of the proposed converter is 96.2% while operating at a maximum output power of 250W.

VIII. CONCLUSION

This article proposes a novel interleaved buck DC-DC converter with high step-down conversion ratios. This converter utilizes a simple auxiliary cell to facilitate soft-switching conditions for the main switching devices. The operational principles and design analysis are discussed. To validate the PLECS simulation results, a laboratory prototype is developed and experimental investigations are performed on a 200 V–60 V converter system. The experimental tests are

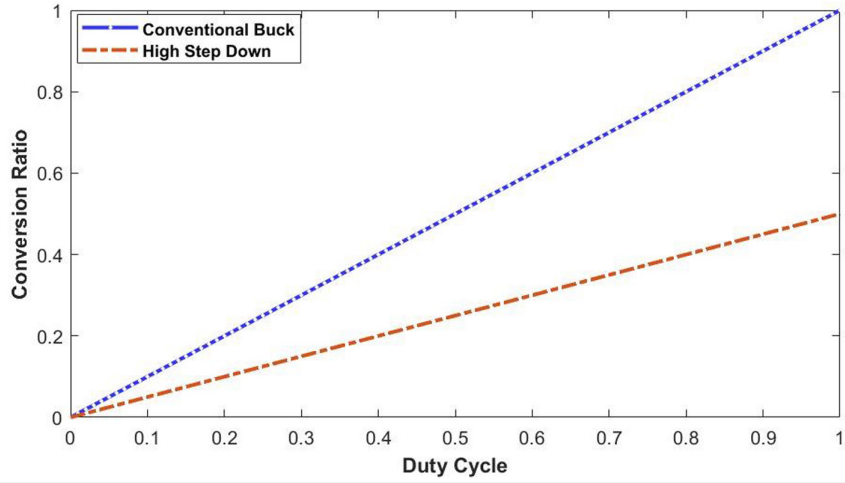

Fig. 21. Duty cycle vs. conversion ratio.

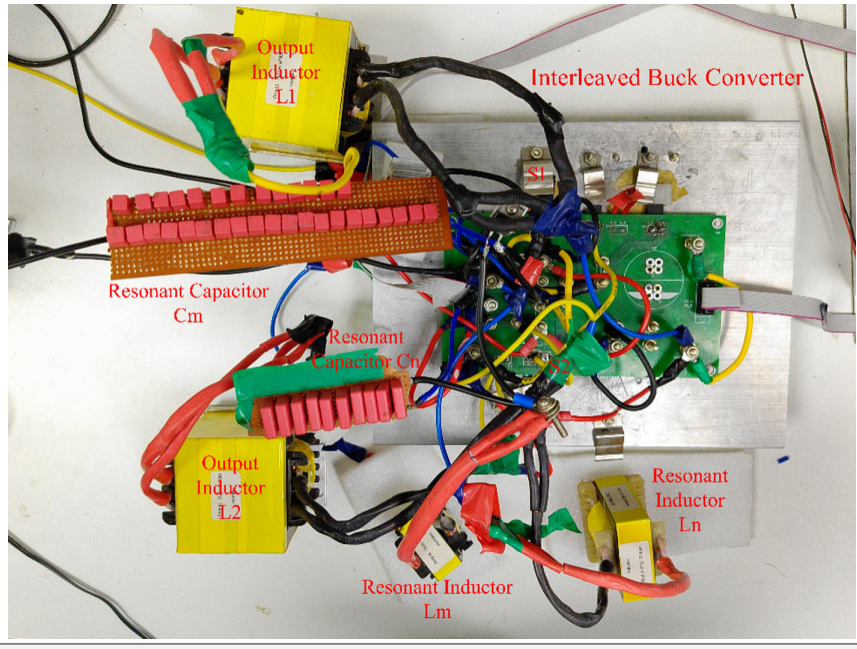

Fig. 22. Hardware prototype of proposed topology.

TABLE III. COMPARISON OF EXISTING CONVERTERS WITH PROPOSED CONVERTER

	NS	NL	NC	ND	f_s(kHz)	V_{in}	V_o	P_o(W)	SS	TD	Efficiency
[5]	4	2	5	2	40	400	25	400	No	13	93.36%
[6]	2	1,1*	2	2	125	100	50	300	Yes	8	95%
[11]	3	1,1*	3	2	50	20	12	72	No	10	96.4%
[12]	3	3	3	2	50	20	12	72	No	11	96.3%
[13]	6	1,2*	2	–	100	48	1.2	400	Yes	11	93.3%
Proposed	2	4	3	4	40	200	60	250	Yes	13	96.13%

f_s, switching frequency; NC, number of capacitors; ND, number of diodes; NL, number of inductors; NS, number of switches; P_o, output power; SS, soft-switching; TD, total device count; V_{in}, input voltage; V_o, output voltage.
*Coupled inductors.

conducted up to 250W output power and confirm the soft-switching ability of the proposed converter without introducing additional stresses. The key advantages of these converters include reduced switching losses, a reduced number of devices, and enhanced efficiency.

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