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A New FGMOS UCCII and SIMO Type Universal Filter Application

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ABSTRACT

A new floating gate MOS (FGMOS) universal current conveyor (UCCII) is proposed to have the properties of simplifier circuit topology, simpler signal processing and wider input swing. Since the FGMOS transistors are used in the proposed UCCII circuit, the number of transistors is reduced and the topology of the circuit is simplified because it is easier to get arithmetic operations in circuits by using FGMOS transistors when compared to conventional MOS transistors. At the same time, using FGMOS differential amplifier structure in the input stage of the FGMOS UCCII circuit increased the input signal swing resulting both an increase in the linearity of the circuit and an improvement in the voltage following properties. A single input multi output (SIMO) type universal filter application is given to show the versatility of the UCCII block. Both the proposed FGMOS UCCII circuit and filter circuit are simulated with SPICE program by using 0.35µm technology parameters. When the simulation results are analyzed it is seen that that the FGMOS UCCII circuit reached the expected improvements according to the MOS equivalent circuit and expected to be used in linearly tunable filters.
Keywords: FGMOS, UCCII, analog, wide range

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Introduction

There has always been a need for differential signals in low-power low-voltage design and designing a circuit for differential signals has enabled versatile applications. So many application examples like filter topologies, multipliers, oscillators are presented in literature [1-4] employing the differential extensions of the second generation current conveyor (CCII) structure. In fact CCII in analog circuit design is very advantageous as a circuit block. Many efficient applications can be made by taking the basic building block of CCII element. In the case of differential input applied circuits, there is a feature that weakens the CCII element, which is a single input node with a high impedance value. The use of multiple CCIIs to solve this problem has been presented as a solution [1]. Another solution is to create more complex CCII structures with differential inputs based on the CCII structure.

Floating Gate MOS (FGMOS) transistors have been used in analog circuit designs in an exciting way in recent years [5-8]. Since FGMOS transistors are widely used in digital circuits, they are already available in standard CMOS technology. For this reason, FGMOS transistors are used by analog designers in more applications nowadays. As a result, FGMOS transistors are used not only in digital circuits but also in analog circuit design. For this purpose, considering the benefits of the FGMOS transistor in voltage following characteristics in current conveyors, the universal current carrier (UCCII), which is designed by taking into account the advantages such as simpler circuit topology in differential current conveyors, has been proposed by using FGMOS transistors.

Universal current carrier structure can be considered as a single circuit block incorporating all current conveyor structures designed like the dual output current conveyor (DOCCII) and differential voltage current conveyor (DVCCII) since the first and second generation current conveyors. In this paper, a new FGMOS UCCII is proposed having the properties of simplifier circuit topology, sim-

pler signal processing and wider input swing. Since the FGMOS transistors are used in the proposed UCCII circuit, the number of transistors is reduced and the topology of the circuit is simplified because it is easier to get arithmetic operations in circuits by using FGMOS transistors when compared to conventional MOS transistors. At the same time, using FGMOS differential amplifier structure in the input stage of the FGMOS UCCII circuit increased the input signal swing resulting both an increase in the linearity of the circuit and an improvement in the voltage following properties. A SIMO type universal filter application is given to show the versatility of the UCCII block. Both the proposed FGMOS UCCII circuit and filter circuit are simulated with SPICE by using 0.35µm technology parameters. When the simulation results are analyzed it is seen that that the FGMOS UCCII circuit reached the expected improvements according to the MOS equivalent circuit and expected to be used in linearly tunable filters.

Rest of the paper is divided into several sections. In the second section, general characteristics of FGMOS transistor are mentioned. In the third section, structure and operation of the proposed FGMOS UCCII circuit is explained. In the fourth and fifth sections, SPICE simulation results of the proposed circuit and filter application are presented, respectively. The last section is conclusion.

FGMOS Transistors

The FGMOS transistor is formed by isolating electrically the gate of a standard MOS transistor at the production stage and by placing multiple inputs on this isolated passage (FG) without any resistive connections. Although there are capacitive connections between the multiple inputs and FG, there is no resistive transition. Since FG is completely surrounded by high resistive material, it is a floating node in terms of dc operating point [5]. The equivalent schematic and equivalent circuit for an n-input n-channel FGMOS transistor are given in Figure 1 and Figure 2, respectively.

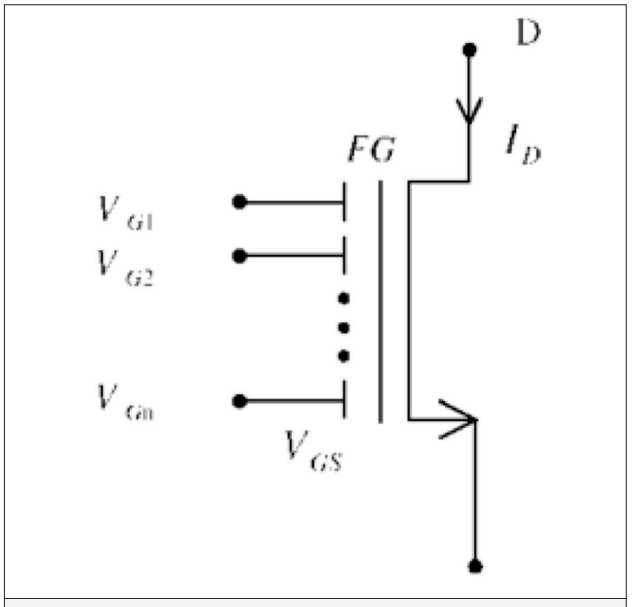

Figure 1. Diagram of a n-input n-channel FGMOS transistor

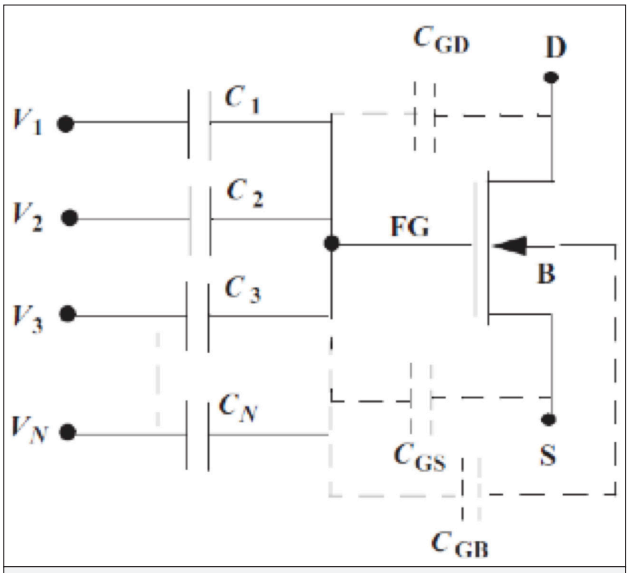

Figure 2. Equivalent circuit of a *n*-input *n*-channel FGMOS transistor

Since the voltages applied to the multiple inputs are capacitively connected to the FG, they control the voltage in the floating gate and tune the current flowing through the MOS transistor channel. The voltage at the FG is given by:

$$V_{FG} = \frac{C_{FGD}V_D + C_{FGS}V_S + C_{FGB}V_B + \sum C_i V_i}{C_T} \quad (1)$$

$$C_T = C_{FGD} + C_{FGS} + C_{FGB} + \sum_{i=1}^{n} C_i \quad (2)$$

The terms V_{FG}, V_D, V_S and V_B in the equations are the floating gate voltage, drain voltage, source voltage and bulk voltage, respectively. C_i are input capacitances where i changes from 1 to n which corresponds the number of multiple inputs. C_{GB}, C_{GS} and C_{GD} are the parasitic capacitances related to bulk, source and drain respectively; and C_T is the sum of C_{GB}, C_{GS}, C_{GD} and C_i.

$$C_i \gg C_{FGD}, C_{FGS}, C_{FGB} \quad (3)$$

Parasitic capacitances are much smaller than the input ones in general and in accordance with the technique in [9], negligible terms of the equation are excluded and gate voltage is equal to the total weight of the input voltages according to the input capacitor values.

Proposed Circuit Description

Universal current carrier is characterized by three high-impedance input terminals (Y_1, Y_2, Y_3), one low-impedance node (X) and four high-impedance output nodes (Z_1, Z_2, Z_1' and Z_2'). Its block scheme is given in Figure 3 and matrix characteristics are summarized in Eq.4.

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Z1} \\ I_{Z2} \\ I_{\overline{Z1}} \\ I_{\overline{Z2}} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_{Z1} \\ V_{Z2} \\ V_{\overline{Z1}} \\ V_{\overline{Z2}} \end{bmatrix} \quad (4)$$

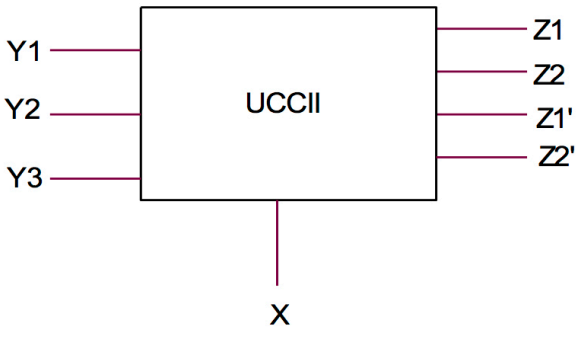

Figure 3. UCCII block representation

Figure 4 shows how UCCII can be obtained from the CCII basic block [1]. In fact, the UCCII structure is similar to the DVCCII structure. An additional Y-node and Z-nodes were added to the structure. In order to obtain other CCII structures from this structure, conjugates of Z nodes were also added to the structure. For example, the classical CCII+ structure can be obtained by taking the Y_1 terminal as the Y node and the Z_1 terminal by the Z node. In addition to other existing CCII structures, some new topologies can also be obtained through this circuit block.

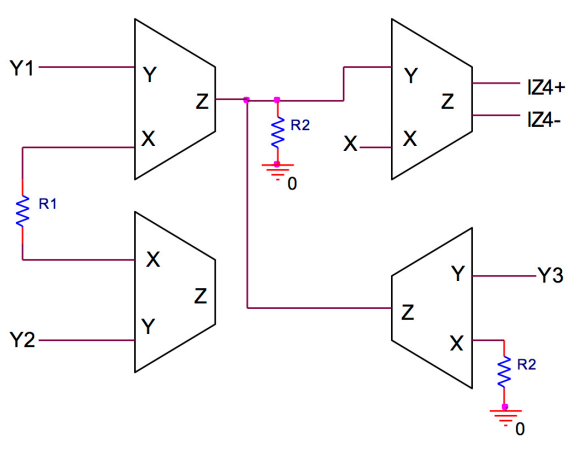

Figure 4. Obtaining UCCII using CCII block

As can be seen in Figure 4;

$$V_X = V_{X4} = V_{Y4} = R_2(I_{Z1} + I_{Z3}) = \frac{R_2(V_{X1}-V_{X2})}{R_1} + \frac{R_2 V_{X3}}{R_3} = \frac{R_2(V_{Y1}-V_{Y2})}{R_1} + \frac{R_2 V_{Y3}}{R_3} \quad (5)$$

If all resistances are chosen equal, then below equation is taken.

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} \quad (6)$$

The proposed FGMOS UCCII circuit is given in Figure 5. As shown in the figure, the differential input stage is constructed with two FGMOS transistors in the proposed circuit. The arithmetic relation between the V_X and $V_{Y1,2,3}$ voltages in the structure is based on the principle of equalizing the current flowing from the FGMOS transistors. For the FGMOS transistors, if the currents are equal, the weighted sum of the voltages applied to the inputs of the FGMOS transistors will be equal. Equal selection of the C_i capacitors connecting the inputs to the floating gate, in other words the FGMOS transistors being the matched transistors, are provided. By providing this feature, $V_{Y1} + V_{Y3} = V_X + V_{Y2}$ equation is obtained between the V_X and $V_{Y1,2,3}$ voltages applied to the inputs of the FGMOS transistors. By adjusting this equation, finally $V_X = V_{Y1}\text{-}V_{Y2} + V_{Y3}$ is obtained.

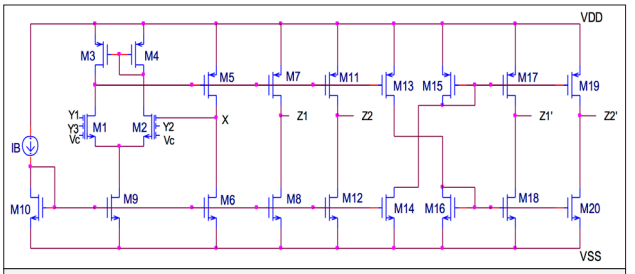

Figure 5. Proposed FGMOS UCCII circuit

Floating Gate MOS transistors in differential pairs have three inputs which are applied through equal sized capacitors, Ci. The input signals of V_{Y1}, V_{Y2}, V_{Y3} and the control voltage V_C are applied to one of the floating gates in the differential pairs. Since the voltage at the gate is less than the input voltage the differential pair transistors can work in saturation even when large signals are applied. This leads to increase the input dynamic swing.

Determining parameters of voltage and current conveying properties are the slopes of related transistors and it is achieved easily by choosing matched transistors.

The parasitic resistances seen at the X and Z terminals and the capacitors seen from the Y terminals (since the R_Y component is very large) can be expressed as follows:

$$R_X = \frac{2}{\frac{C_i}{C_T} g_{m2} \left| g_{m5}\left(g_{ds1} + \frac{C_{GD}}{C_T} g_{m1} + g_{ds3}\right)^{-1} // r_{o6} \right|} \quad (7)$$

$$R_{Z1} = r_{o7} // r_{o8},\ R_{Z2} = r_{o11} // r_{o12},\ R_{Z1'} = r_{o17} // r_{o18},\ R_{Z2'} = r_{o19} // r_{o20} \quad (8)$$

$$C_Y = \frac{2}{3}(WLC_{OX}) \quad (9)$$

Simulation Results

The proposed FGMOS UCCII structure has been simulated in the SPICE program with 0.35 µm TSMC technology parameters. Supply voltage is taken as ± 1.5V while V_C voltage is taken as control voltage. The bias current is chosen as I_B = 125µA. The dimensions of the n-type transistors are taken as W / L = 2.1

µm / 0.7 µm and the p-type transistors are taken as W / L = 10.5 µm / 0.7 µm. The C_{FGD} and C_{FGS} capacitor values are calculated as 0.6fF and 5fF and the input capacitor values are chosen as C_i = 50fF. The compensation capacitor of 20fF is applied between the drain and gate terminals of the M7 and M11 transistors.

Figure 6-8 show the DC voltage transfer characteristics of the proposed circuit with respect to $V_{Y1, Y2, Y3}$ input DC voltages. DC voltage $V_{Y1, Y2, Y3}$ is swept between -1.5V and 1.5V while the DC voltage V_X is plotted. In Figure 6-8 while V_{Yi} is -1.5V, V_X takes -1.5V, 1.43V and -1.49V, respectively. While V_{Yi} is 1.5V, V_X takes 1.41V, -1.49V and 1.4V, respectively. As it is seen from these values, input swing is almost equal to the supply voltages.

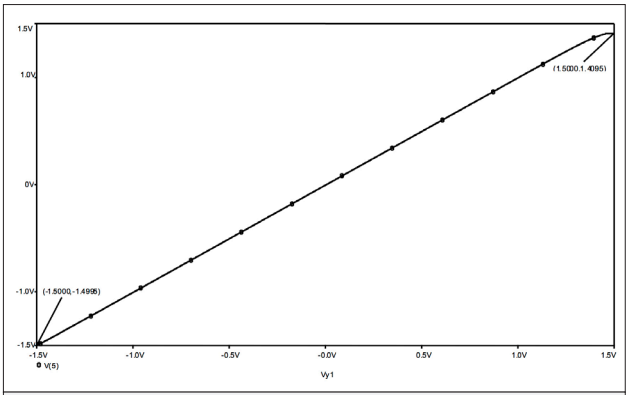

Figure 6. FGMOS UCCII DC voltage transfer characteristics (V_X-V_{Y1})

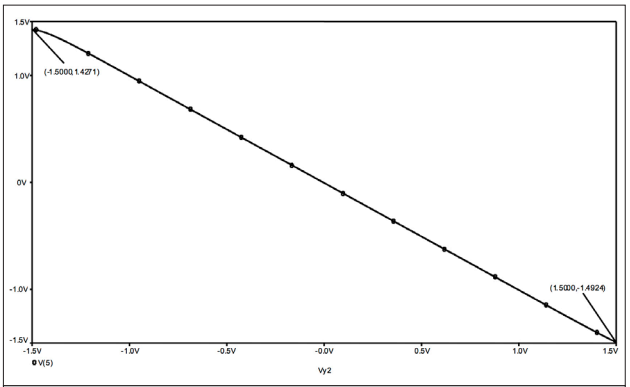

Figure 7. FGMOS UCCII DC voltage transfer characteristics (V_X-V_{Y2})

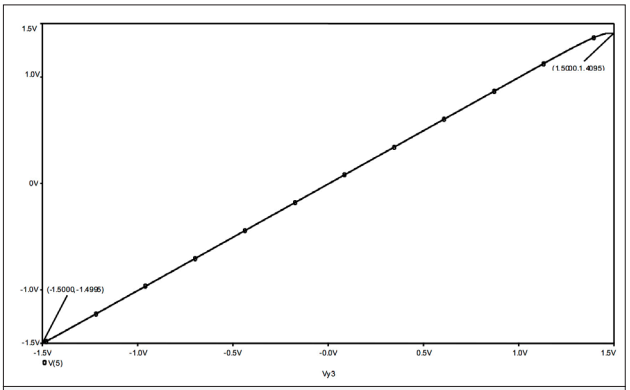

Figure 8. FGMOS UCCII DC voltage transfer characteristics (V_X-V_{Y3})

Figure 9 shows the DC current transfer characteristics of the FGMOS UCCII structure. As can be seen from the figure, the I_X current was swept between -10µA and 10µA while the DC output currents I_{Z1}, I_{Z2}, $I_{Z1'}$ and $I_{Z2'}$ currents are plotted. Between the input and output currents $I_X = I_{Z1} = I_{Z2}$ and $-I_X = I_{Z1'} = I_{Z2'}$ relations are obtained.

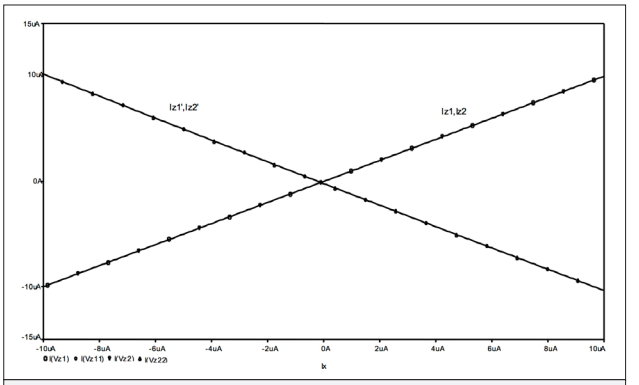

Figure 9. FGMOS UCCII DC current transfer characteristics

Figure 10 shows the AC voltage transfer characteristics of the FGMOS UCCII structure. In the AC voltage transfer characteristics, the 3dB frequency value is approximately 200MHz for V_{Y1}, V_{Y3} and 350MHz for V_{Y2}.

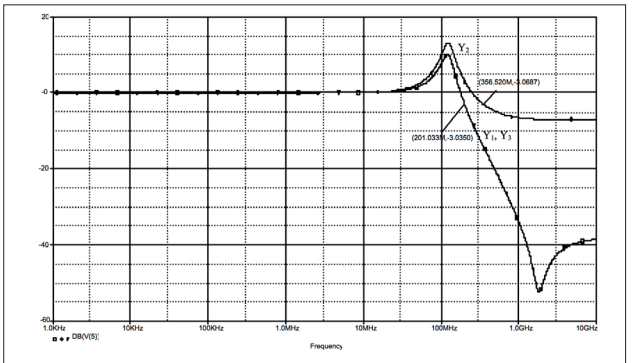

Figure 10. FGMOS UCCII AC voltage transfer characteristics (V_X-$V_{Y1,2,3}$)

Figure 11 shows the AC current transfer characteristics of the FGMOS UCCII structure. In the AC current transfer characteristics, the 3dB frequency value is approximately 340MHz.

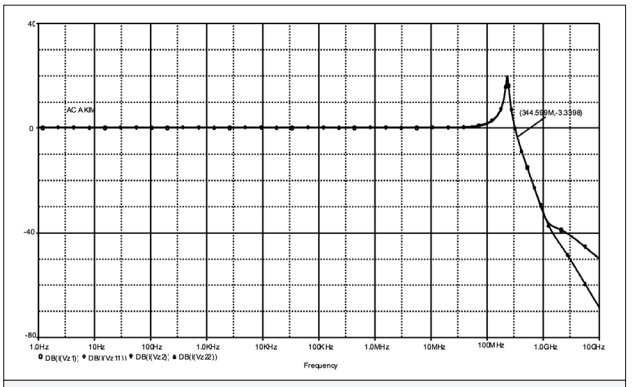

Figure 11. FGMOS FDCCII AC current transfer characteristics (I_X-$I_{Z1,2,1',2'}$)

When UCCII structure is formed by conventional MOS transistors, 31 transistors are used except for bias current [10]. When this structure is examined, it is seen that 6 transistors are used in the input stage to obtain $V_X = V_{Y1} - V_{Y2} + V_{Y3}$ correlation between X and Y nodes. In the proposed FGMOS UCCII structure, a total of 20 transistors, including bias current, are used. At this point, the number of transistors is reduced to three by using FGMOS transistors at the input stage which provides the correlation between the X and Y nodes in order to take advantage of the simplicity of providing arithmetic operations. Also the voltage following characteristics of the UCCII structure are improved with the linearity improvement of the FGMOS differential amplifier. It is known that the input swing of differential amplifier is increased by a factor of C_T / C_i by using FGMOS transistors instead of conventional MOS transistors [11, 12]. In addition, new Y terminals can be added by only increasing the number of input terminals of the FGMOS transistors used, without adding a new transistor to the UCCII structure. This shows the flexibility of using FGMOS transistors in circuit blocks with arithmetic operations.

The performance criteria obtained by the SPICE simulation program of the proposed FGMOS UCCII structure is summarized in Table 1.

Table 1. FGMOS and MOS UCCII circuits performance criteria

	FGMOS UCCII	MOS UCCII [10]
Supply voltage	±1.5V	±3V
Bias current	125μA	300μA
Input linearity swing (V_X-V_{Y1}, V_X-V_{Y3})	(-1.5V, 1.38V)	NA
Input linearity swing (V_X-V_{Y2})	(-1.49V, 1.4V)	NA
Maximum input signal (@THD=%5)	±1.36V	NA
Parasitic resistance (X, Y, Z)	405Ω, 14GΩ, 114kΩ	4mΩ (X)
-3dB bandwidth (V_X/V_{Y1}, V_X/V_{Y2}, V_X/V_{Y3})	280MHz, 436MHz, 280MHz	64MHz
-3dB bandwidth (I_Z/I_X)	180MHz	73.5MHz

FGMOS: Floating Gate MOS; UCCII: Universal Current Conveyor

SIMO Type Universal Filter Application

One input multi-output filter structure obtained using the FGMOS UCCII circuit is given in Figure 12 [13]. The structure consists of three UCCII and four passive elements. All passive elements are grounded, which gives an advantage for the integrated circuit design.

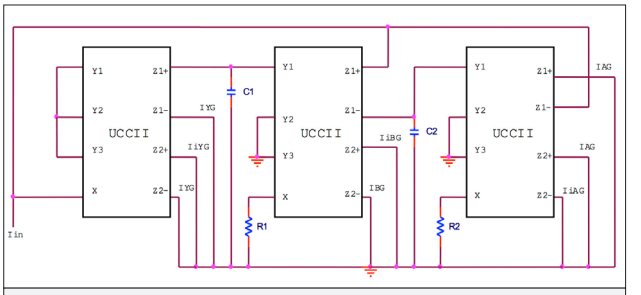

Figure 12. One input multi-output filter structure obtained using FGMOS UCCII circuit

The transfer functions of the filter structure are as follows.

$$\frac{I_{LP}}{I_{in}} = \frac{-I_{iLP}}{I_{in}} = \frac{1}{1+sC_2R_2+s^2R_1R_2C_1C_2} \quad (10)$$

$$\frac{I_{BP}}{I_{in}} = \frac{-I_{iBP}}{I_{in}} = \frac{sC_2R_2}{1+sC_2R_2+s^2R_1R_2C_1C_2} \quad (11)$$

$$\frac{I_{HP}}{I_{in}} = \frac{-I_{iHP}}{I_{in}} = \frac{s^2R_1R_2C_1C_2}{1+sC_2R_2+s^2R_1R_2C_1C_2} \quad (12)$$

The angular cut-off frequency and the quality factor are the same for all filters and are as follows.

$$\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (13)$$

$$Q_0 = \sqrt{\frac{R_1C_1}{R_2C_2}} \quad (14)$$

Figure 13 shows the output curves of one input multi-output filter structure using the UCCII structure. In order to obtain f_0 = 1MHz, Q = 1 / √2 at the curves shown in Figure 13 according to equation (13), R_1, R_2, C_1 and C_2 are chosen as R_1 = 22kΩ, R_2 = 44kΩ and $C_1 = C_2$ = 5pF.

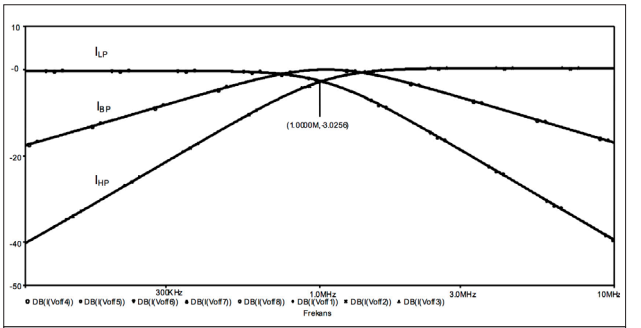

Figure 13. Output curves of one input multiple output filter structure performed with the FGMOS UCCII circuit

In order to examine the large signal behavior of one input multi-output filter structure obtained with FGMOS UCCII, an input signal of 1MHz sinusoidal with 200μA peak-to-peak amplitude is applied and the output currents are examined. The resulting output curves are shown in Figure 14.

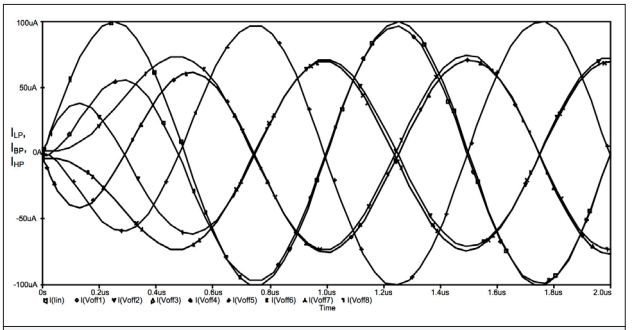

Figure 14. Large signal behavior of one input multi-output filter structure performed with the FGMOS UCCII circuit

Conclusion

Since the FGMOS transistors are used in the proposed UCCII circuit, the number of transistors is reduced and the topology of the circuit is simplified because it is easier to get arithmetic operations in circuits by using FGMOS transistors when compared to conventional MOS transistors. At the same time, using FGMOS differential amplifier structure in the input stage of the FGMOS UCCII circuit increased the input signal swing resulting both an increase in the linearity of the circuit and an improvement in the voltage following properties. The FGMOS UCCII circuit is handled with the CMOS equivalent and the simulation results are given in a tabular form. When the results given are analyzed, it is seen that the FGMOS UCCII circuit reached the expected improvements according to the MOS equivalent circuit.

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Conflict of Interest: The authors have no conflicts of interest to declare.

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