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A DTMOS based Four-Quadrant Analog Multiplier

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ABSTRACT

One of the most common circuit structures, four-quadrant analog multipliers (FQAM) are frequently preferred for modulation, phase shifting, adaptive filtering, neural network applications. In this study, an FQAM design is presented using dynamic threshold voltage MOSFET (DTMOS) technology. Various analyses were performed to evaluate the function of the proposed multiplier. Power consumption is limited by selecting ±0.2 V supply voltage. The power consumption of the circuit is calculated as 37 nW. The maximum amplitude of the input signal is 0.1 V. The bandwidth of the multiplier is 3.23 MHz. The total harmonic distortion (THD) of the output signal at the maximum value of the input signal and at a frequency of 100 kHz is around 1.2%. Intermodulation products were calculated to analyze the linearity of the circuit. The changes in DC and AC transfer characteristics according to temperature changes were investigated. Monte Carlo analysis was performed to verify the circuit's robustness against variation of the circuit parameters. In summary, low power consumption and THD, and insensitive of temperature variations are the outstanding features of the circuit when compared with the literature.

Keywords: Analog multipliers, DTMOS, low power, low voltage

Introduction

FQAMs are considered as basic circuit blocks used in electronic and communication disciplines such as amplitude modulation, frequency doubling, modulators, adaptive filters, neural networks, and sensor applications.

Multiplication of two continuous analog signals is accomplished with analog multiplier circuits. The mathematical output expression of the multiplier is shown as $z=Kxy$. Here, x and y denote the sign and K denotes an appropriate size constant. The multipliers are classified according to the operating region of the transistors (weak inversion [1-3], strong inversion [4, 5], saturation [6-10] and linear [11-13] and the polarization of the input signal (one-quadrant, two-quadrant, four-quadrant). It is also classified as current or voltage mode according to the input signal mode.

Mobile devices such as smartphones and tablets, which are increasingly used today and are an indispensable part of our lives, are powered by batteries. Given the size and weight of the batteries, the capacity of the batteries used in these devices is limited. The limited capacity of the battery requires efficient use of energy. In late years, many multipliers have been offered with low power, high performance circuit techniques. The studies of analog multiplier can be classified as: Weak-inversion region [3, 14, 15], DTMOS technology [16-18], Floating-gate MOSFET (FGMOS) technology [19-22], subthreshold region [23-25] and bulk driven [26-28].

Liu and Liu [1] have been introduced an analog multiplier that consists of the MOSFETs that operate in the weak inversion region. The multiplier is based on the exponential characteristic of the MOSFETS. 0.35 µm CMOS process parameters were used for performing the simulations. According to the simulation results, for V_{DD}=1.5 V, the bandwidth of 268 kHz, THD of around 4.2%, linearity error of 3.2%, the input range of 120 mV, and power consumption of 6.7 µW have been achieved.

Babacan [16] has been suggested a multiplier using the DTMOS technology. 0.18 µm CMOS technology parameters were performed for simulations. In this study, 18.4 nW power consumption was provided under ± 0.2V supply voltage. The bandwidth is 1.11 MHz for V1 input and 39.5 kHz for V2 input.

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Panigrahi and Paul [14] have presented a FQAM that includes bulk driven MOS devices. The MOSFETs operates in the weak invasion region. 180 nm CMOS technology parameters have been accomplished for simulations. In the simulation results, under 0.5 V supply voltage, the bandwidth of 221 kHz, THD of about 5%, and power consumption of 714 nW were achieved.

Zamora-Mejia et al. [29] have presented a FQAM by using the bulk-driven technique. The bandwidth is 50 MHz and THD is lower than 1%. The power consumption of the core circuit is 660μW. The ONSemi 0.50μm CMOS standard technology has been used to simulate and fabricate the multiplier circuit.

Hashiesh et al. [7] have suggested a current-mode FQAM by using squarer cell. According to the simulation results, the power consumptions are 0.72 mW and 1.85 mW, the input current ranges are ±60 μA and ±1 V, the bandwidths are 31 MHz and 25.34 MHz, the linearity errors are 3.9% and 4.1% for the current mode and voltage mode topologies, respectively.

Boonchu and Surakampontorn [30] have proposed a CMOS voltage-mode FQAM built on diode-connected MOS transistor. According to the simulation results, the bandwidth of 30 MHz, the input range is +400 mV with the linearity error of 0.8% and the THD of 0.62% and the power consumption of 1.26 mW.

In this article, a low power consumption DTMOS based FQAM operating under low voltage is proposed. The modified circuit topology was first introduced in 2005 by Boonchu and Surakampontorn [31]. The multiplication function of the circuit is built on the quadratic characteristic of the MOS transistors. The MOS devices operates the saturation region. The LTspice Program (Analog Devices, Massachusetts, MA, USA) with 45 nm PTM model parameters under ±0.2 V supply voltage has been used for the simulations. The DC transfer characteristic is introduced to depict the four-quadrant multiplier function. AC transfer characteristics, THD and temperature sensitivity were investigated. It has been established to be used as a basic analog circuit such as amplitude modulator and frequency doubler. Intermodulation products are calculated to show the linearity of the circuit. Monte Carlo analysis is carried out to verify the reliability and robustness of the FQAM.

The paper consists of sections that described as follows: In section 2, an analog multiplier circuit is introduced. Simulation results for assessing the performance of the proposed FQAM are given in Chapter 3. The conclusion of the paper is presented in Chapter 4.

Four-Quadrant Analog Multiplier Using Dynamic Threshold Voltage MOSFET

The use of mobile devices powered by batteries, such as smartphones and tablets, is becoming increasingly common. Battery capacity is limited due to limitations in the size and weight of many mobile devices. Therefore, efficient use of energy is essential. Researchers have begun to work more on low power, high-performance circuit techniques for power consumption management.

An attempt is made to reduce the supply voltage to limit power consumption. The supply voltage cannot be reduced below a certain level, as it may cause power problems in the standby condition and circuit speed problems in the memory elements. A MOSFET with a dynamic threshold voltage can be used to overcome these problems. Using DTMOS circuit technology, high performance can be achieved under low supply voltage in low-voltage MOSFET and VLSI circuits [32-37]. DTMOS is obtained by connecting the body and gate of the MOSFET together as shown in Figure 1.

The expression of threshold voltage is given below.

$$V_{TH} = V_{T0} + \gamma\left(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0}\right) \quad (1)$$

where DIBL effect is ignored. V_{TH} is threshold voltage, V_{SB} is the source-to-body voltage. V_{T0} is the zero body bias threshold voltage. V_{T0} is defined by

$$V_{T0} = V_{FB} + \phi_0 + \gamma\sqrt{\phi_0} \quad (2)$$

V_{FB} is the flat band voltage and γ is the body effect factor. It is defined by

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}} \quad (3)$$

ε_{si} represents dielectric permittivity of silicon, N_A is the substrate doping, C_{ox} is the oxide capacitance for unit area. For simplification, ϕ_0 is accepted as $\phi_0 = 2\,\phi_F$.

Using DTMOS technology, the junction width is reduced and consequently causes a decrease in the charge density of the depletion region. This allows V_{TH} to be reduced. In the case of reverse polarity, the width of the depletion region increases, so the increase in charges results in an increase in V_{TH}. In the case of forwarding polarity, V_{TH} will be low. When the transistor goes off, V_{TH} increases, resulting in low leakage current. Thus, V_{TH} is

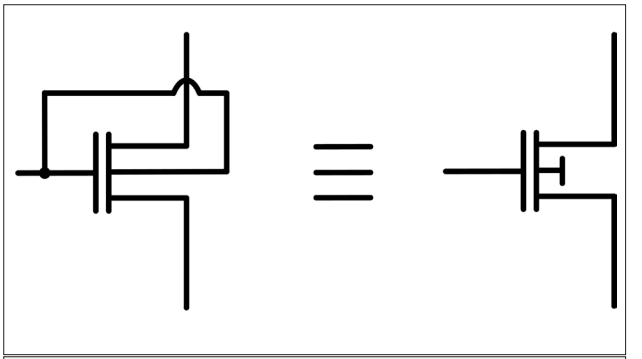

Figure 1. DTMOS circuit topology and symbol [38]

dynamically changed according to the gate input, that is, according to the operating state of the circuit.

The analog multiplier circuit studied in this paper was firstly presented by Boonchu and Surakampontorn in 2005 [31]. The fundamental circuit of the multiplier is shown in Figure 2. The circuit is built on square law characteristic of MOS transistors that operate in the saturation region. The current sources I_{DD1} and I_{DD2} provide the bias currents and I_{DD1} = 0.01μA, I_{DD2} = *0.5μA*.

The bias current I_{DD1} is equal to the summing of the drain currents of the transistor M1-M2 and expressed in equation (4).

$$I_{DD1} = I_{d1} + I_{d2} = K_n\left(V_{g3} - V_1 - V_{Tn}\right)^2 + K_n\left(V_{g3} - V_2 - V_{Tn}\right)^2 \quad (4)$$

where V_{Tn} is the threshold voltage and K_n is the transconductance of the NMOS transistor. $K_n = \mu C_{ox} W/L$, μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, is the channel width, and is the channel length.

The gate voltage of transistor M3 V_{g3} can be expressed as in equation (5).

$$V_{g3} = \frac{V_1 + V_2}{2} + V_{Tn} + \sqrt{\frac{I_{DD1}}{2K_n}}\sqrt{1 + \frac{K_n}{2I_{DD1}}(2V_1V_2 - V_1^2 - V_2^2)} \quad (5)$$

Maclaurin's series of the function of the form $f(x) = \sqrt{1+x}$ as follows:

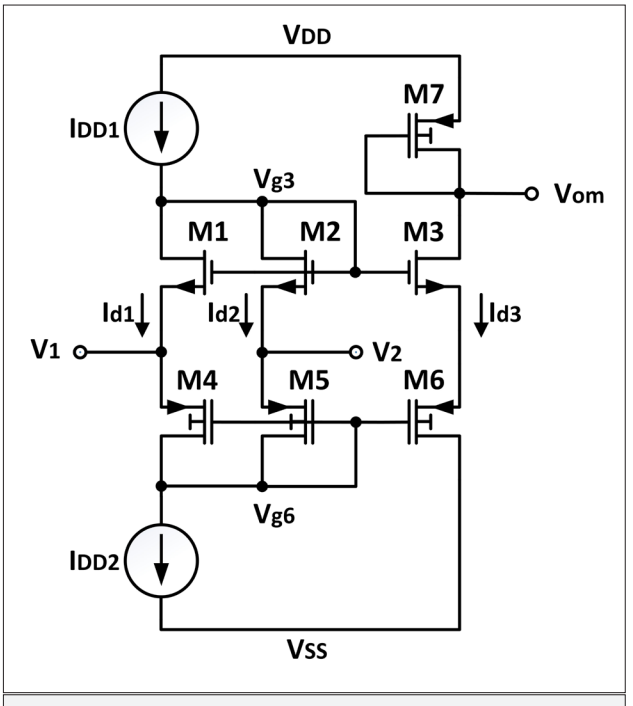

Figure 2. The basic amplifier circuit

$$\sqrt{1+x} = 1 + \frac{x}{2} - \frac{x^2}{8} + \frac{x^3}{16} + \cdots \quad (6)$$

The first and second term of the series is equal to function approximately, and the form $\sqrt{1+x} \cong 1 + \frac{x}{2}$, for is used and the equation (5) can be written below.

$$V_{g3} = \frac{V_1 + V_2}{2} + V_{Tn} + \sqrt{\frac{I_{DD1}}{2K_n}}\left[1 + \frac{K_n}{2I_{DD1}}(2V_1V_2 - V_1^2 - V_2^2)\right] \quad (7)$$

The gate voltage of transistor M6 V_{g6} is given by

$$V_{g6} = \frac{V_1 + V_2}{2} - |V_{Tp}| - \sqrt{\frac{I_{DD2}}{2K_p}}\left[1 + \frac{K_p}{2I_{DD2}}(2V_1V_2 - V_1^2 - V_2^2)\right] \quad (8)$$

where V_{Tp} is the threshold voltage and K_n is the transconductance of the PMOS transistor. The output voltage V_{om} is written in the form of V_{g3} and V_{g6} as

$$V_{om} = V_{DD} - |V_{Tp}| - \frac{\sqrt{K_n}}{\sqrt{K_n} + \sqrt{K_p}}\left[V_{g3} - V_{g6} - V_{Tn} - |V_{Tp}|\right] \quad (9)$$

The output voltage of the circuit, V_{om} can be expressed by substituting equations (7), (8) into (9).

$$V_{om} = V_{DD} - |V_{Tp}| - \frac{\sqrt{K_n}}{\sqrt{K_n} + \sqrt{K_p}}\left[\sqrt{\frac{I_{DD1}}{2K_n}} + \sqrt{\frac{I_{DD2}}{2K_p}} + (2V_1V_2 - V_1^2 - V_2^2)\frac{\sqrt{2}}{4}\left(\sqrt{\frac{K_n}{I_{DD1}}} + \sqrt{\frac{K_p}{I_{DD2}}}\right)\right] \quad (10)$$

Equation (10) indicates that the circuit performs the multiplication function of the input signals V_1 and V_2. But the output voltage V_{om} contains the second order terms of the input voltages V_1 and V_2.

Higher-order terms cause an error in the multiplication function. The complete circuit of DTMOS based FQAM, where this error is eliminated, is given in Figure 3. Transistors M1-M3 and M8-M10 have the same dimensions with the transconductance K_n, M4-M7 and M11-M14 are identical with the transconductance K_p. Using equation (10), the output voltages V_{om1} and V_{om2} of each circuit can be obtained as follows:

$$V_{om1} = V_{DD} - |V_{Tp}| - \frac{\sqrt{K_n}}{\sqrt{K_n} + \sqrt{K_p}}\left[\sqrt{\frac{I_{DD1}}{2K_n}} + \sqrt{\frac{I_{DD2}}{2K_p}} + (2V_1V_2 - V_1^2 - V_2^2)\frac{\sqrt{2}}{4}\left(\sqrt{\frac{K_n}{I_{DD1}}} + \sqrt{\frac{K_p}{I_{DD2}}}\right)\right] \quad (11)$$

$$V_{om2} = V_{DD} - |V_{Tp}| - \frac{\sqrt{K_n}}{\sqrt{K_n} + \sqrt{K_p}}\left[\sqrt{\frac{I_{DD3}}{2K_n}} + \sqrt{\frac{I_{DD4}}{2K_p}} + (-2V_1V_2 - V_1^2 - V_2^2)\frac{\sqrt{2}}{4}\left(\sqrt{\frac{K_n}{I_{DD3}}} + \sqrt{\frac{K_p}{I_{DD4}}}\right)\right] \quad (12)$$

Finally, by subtracting between V_{om1} and V_{om2}, the output voltage V_{out} of the circuit is carried out by

$$V_{out} = V_{om1} - V_{om2} = V_1V_2\frac{\sqrt{2K_n}}{\sqrt{K_n} + \sqrt{K_p}}\left(\sqrt{\frac{K_n}{I_{DD1}}} + \sqrt{\frac{K_p}{I_{DD2}}}\right) \quad (13)$$

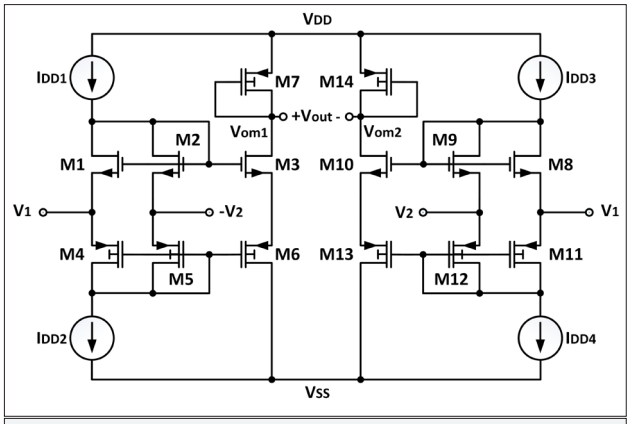

Figure 3. DTMOS based FQAM

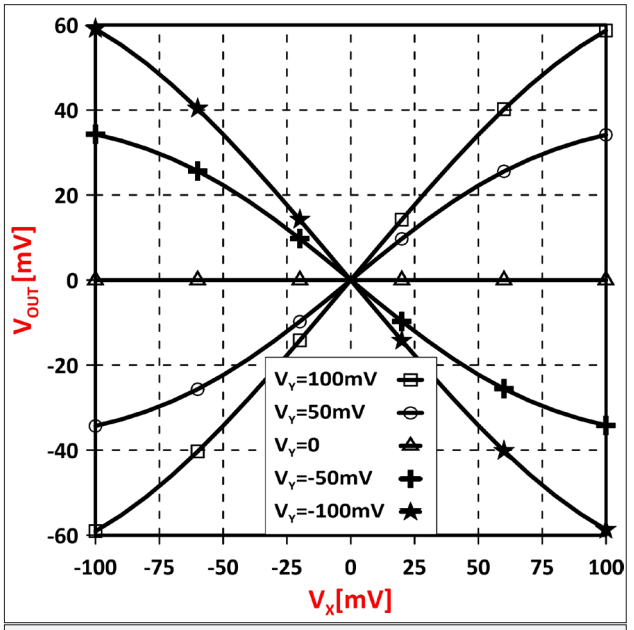

Figure 4. DC characteristic (V_X terminal.

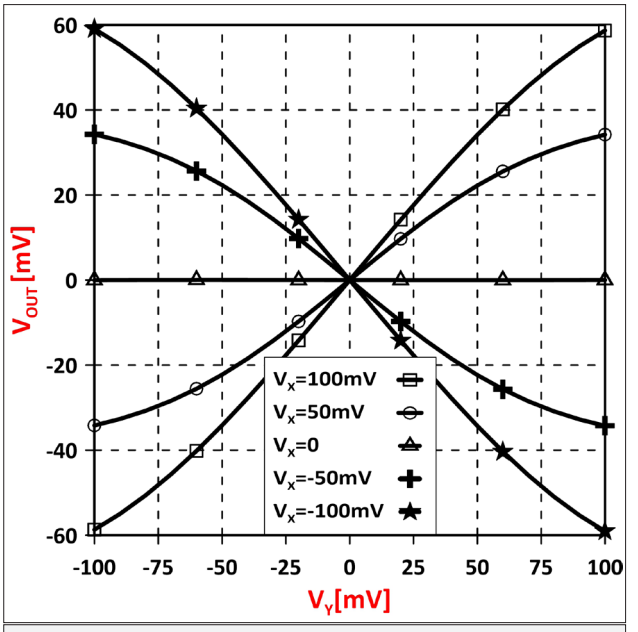

Figure 5. DC characteristic (V_Y terminal)

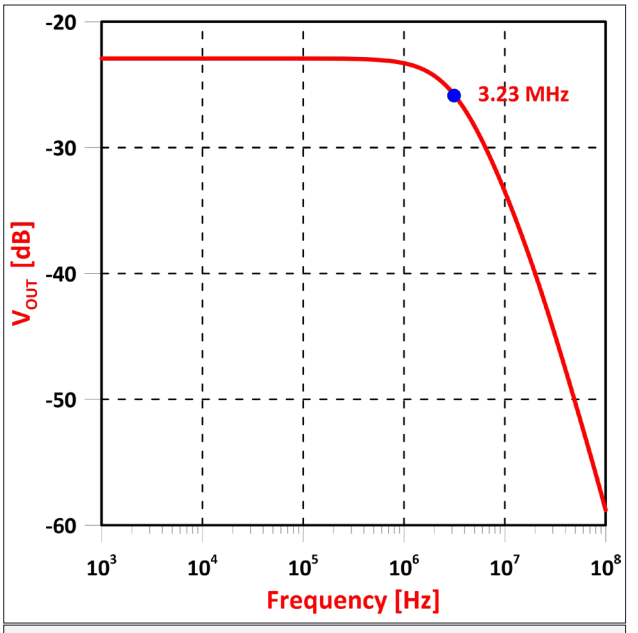

Figure 6. AC characteristic

The output voltage can be scaled by K_n, K_p, I_{DD1} and I_{DD2} as indicated by (13). The bias currents are $I_{DD1} = I_{DD3} = 0.01\mu A$, $I_{DD2} = I_{DD4} = 0.5\mu A$.

Simulation Results

Various simulation results are presented in this part of the paper to evaluate the performance of the proposed FQAM. The LTspice program (Analog Devices, Massachusetts, MA, USA) with Predictive Technology Model (PTM) 45 nm Level 54 CMOS process model parameters were executed for simulations. The supply voltage is ±0.2V. The dimensions of the MOS transistors is tabulated in Table 1.

The DC transfer characteristics of the proposed FQAM are given in Figures 4 and 5. Figure 4 shows the DC transfer curve between V_{out} and V_1. In this way, V_1 ranges from –100 mV to 100 mV, while V_2 ranges from -100 mV to 100 mV in 50 mV steps. Figure 5 shows the DC transfer curve between V_{out} and V_2. In this curve, V_2 ranges from –100 mV to 100 mV, while V_1 ranges from -100 mV to 100 mV in 50 mV steps.

The AC transfer characteristic curve of the circuit is presented in Figure 6. Accordingly, the -3 dB bandwidth is 3.23 MHz. The simulation was performed by applying a 100 mV DC signal to V_1 input of the circuit and 100 mVp-p AC signal to V_2 input.

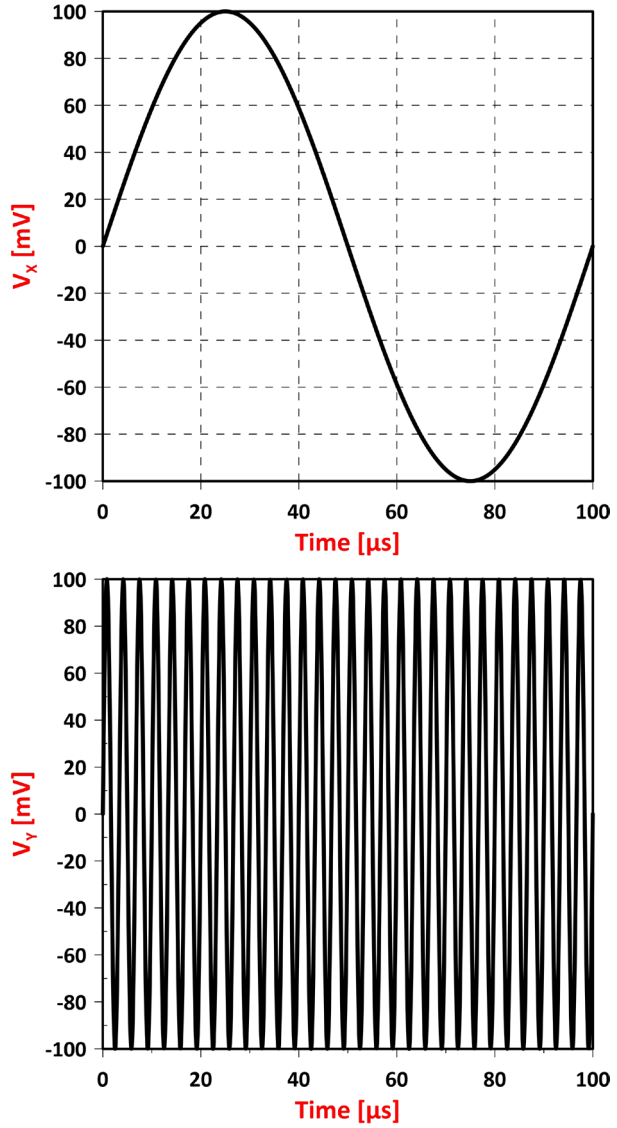

Figure 7. Input waveforms of the modulator

Table 1. Aspect ratio of the MOS transistors.

Transistor	W	L
M1 – M3, M8 – M10	90 nm	90 nm
M4 – M7, M11 – M14	27 µm	90 nm

(W: width, L: length)

To verify the use of the proposed FQAM as an amplitude modulator, two sinusoidal signals of 100 mV amplitude were applied to inputs V_1 and V_2 at frequencies 10 kHz and 300 kHz respectively. The waveforms of the input signals are shown in Figure 7. The output waveform of the amplitude modulator is shown in Figure 8.

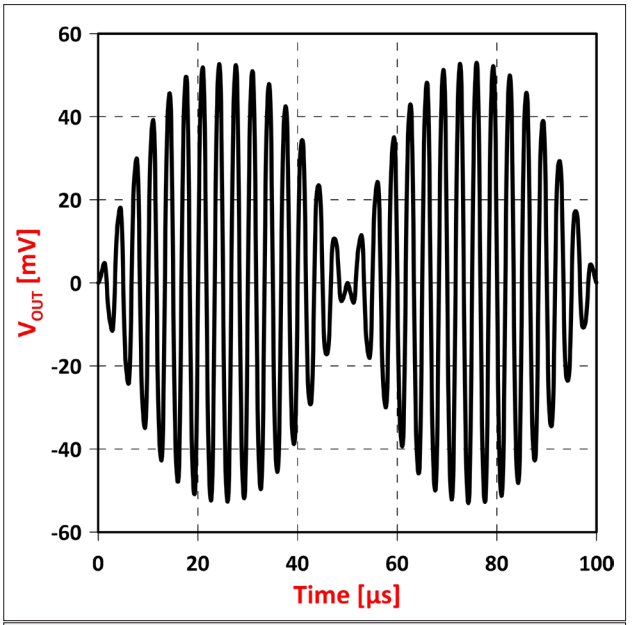

Figure 8. Output waveform of the modulator

Intermodulation distortion is an important performance criterion for analog multipliers. Ideally, an analog multiplier should not have intermodulation products. Intermodulation products were obtained by applying two sinusoidal signals to the inputs of the multiplier at frequencies of 10 kHz and 300 kHz and amplitude of 100 mV. Table 2 shows the 2nd, 3rd, 4th and 5th degree intermodulation products of the multiplier. Furthermore, the frequency spectrum of the output of the proposed FQAM is given in Figure 9.

As an indicator of linearity for analog multipliers, THD is one of the key parameters. Ideally, it is desirable that the THD of an analog multiplier is zero. In practical applications, a THD of less than 5% is an acceptable limit. In order to evaluate the linearity of the proposed multiplier, the variation of the THD with the amplitude and frequency of the input signal was investigated.

THD simulation was carried out by applying an AC and DC signal to V_1 and V_2 input, respectively. The input signals have 100 mV amplitude. The simulation was repeated for three sinusoidal signals at frequencies f_1=100 Hz, f_2=10 kHz and f_3=1 MHz. As a result, the variation of THD as a function of the amplitude and frequency of the input signal is shown in Figure 10. THD is less than 6.34% when the input signal amplitude reaches the highest 200 mV.

To test the frequency multiplier function of the multiplier, a sinusoidal signal of 100 mV amplitude and 10 kHz frequency was applied to both inputs of the multiplier. The accuracy of the frequency folding function is shown in Figures 11 and 12.

The effect of temperature variation on the DC and AC transfer characteristics of the proposed multiplier was analyzed. The DC characteristic change is shown in Figure 13 and the AC characteristic change is shown in Figure 14 at temperature T=0°C, T=50°C and T=100°C.

Table 2. Intermodulation products.

Order	Harmonics [kHz]	Fourier Components	Normalized Fourier Components (dB)	Intermodulation Products [kHz]	Fourier Components	Normalized Fourier Components (dB)
2	20	2.33×10^{-16}	-51.37	290	3.19×10^{-11}	0
	600	2.06×10^{-16}	-51.92	310	3.19×10^{-11}	0
3	30	1.23×10^{-16}	-54.15	320	5.28×10^{-14}	-27.81
	900	3.78×10^{-14}	-29.27	590	1.93×10^{-16}	-52.18
				610	2.90×10^{-11}	-50.42
4	40	1.79×10^{-16}	-52.51	330	2.26×10^{-12}	-11.51
				580	4.10×10^{-16}	-48.92
				620	3.28×10^{-16}	-49.88
	1200	3.66×10^{-16}	-49.41	890	2.36×10^{-12}	-11.31
				910	2.37×10^{-12}	-11.30
5	50	4.95×10^{-16}	-48.09	340	7.07×10^{-15}	-36.55
				630	4.64×10^{-16}	-48.38
				880	1.37×10^{-14}	-33.69
	1500	4.94×10^{-15}	-38.11	920	1.34×10^{-14}	-33.78
				1190	6.90×10^{-17}	-56.66
				1210	3.30×10^{-16}	-49.86

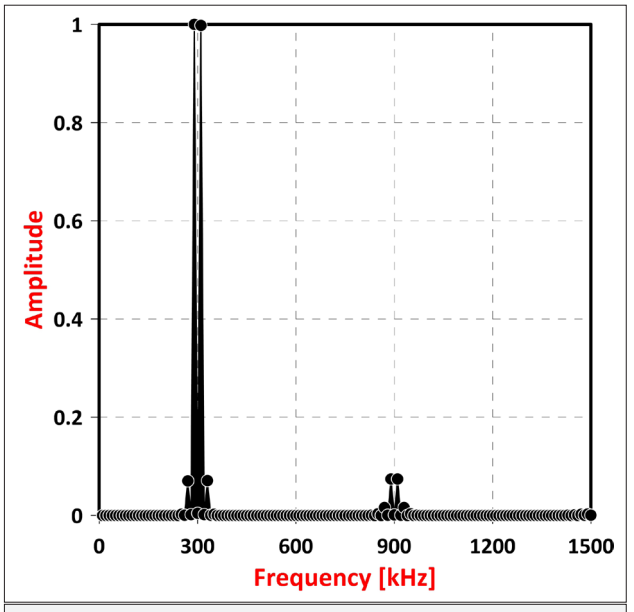

Figure 9. Frequency spectrum of the modulator

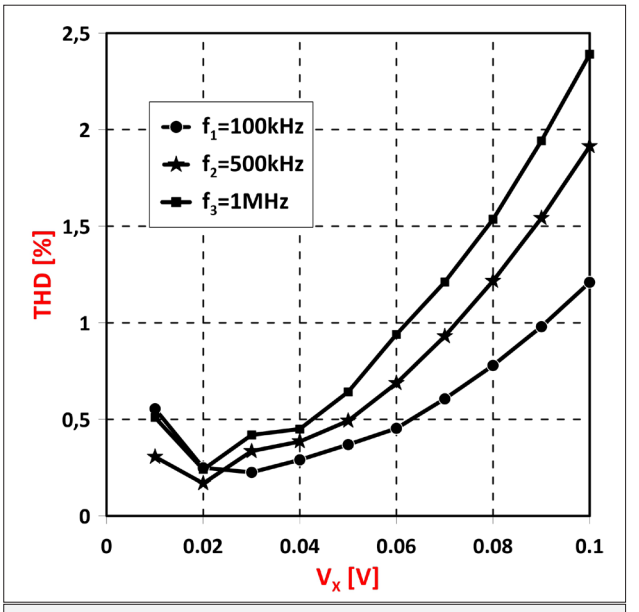

Figure 10. Variation of THD

Monte Carlo analysis for the circuit given in Figure 3 was carried out with 400 operations. This analysis was made with a 10% change in W dimensions. According to Figure 15, the average value of the bandwidth is 3.21 MHz. The minimum and maximum bandwidth values are 2.91 MHz and 3.54 MHz, respectively. In addition to 400 operations, Monte Carlo analysis of the analog multiplier, a 10% variation of parameters such as width (W), V_{TH} and t_{ox} (gate oxide thickness) was analyzed. According to the Monte

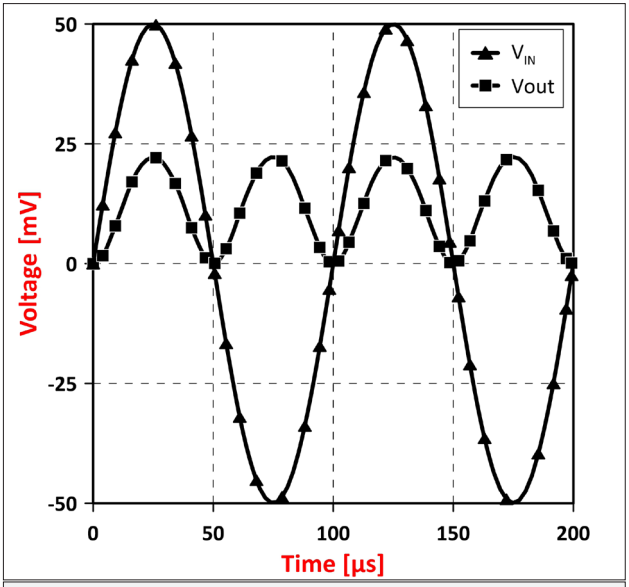

Figure 11. Input (V_{IN}) and output (V_{OUT}) waveforms of the frequency doubler

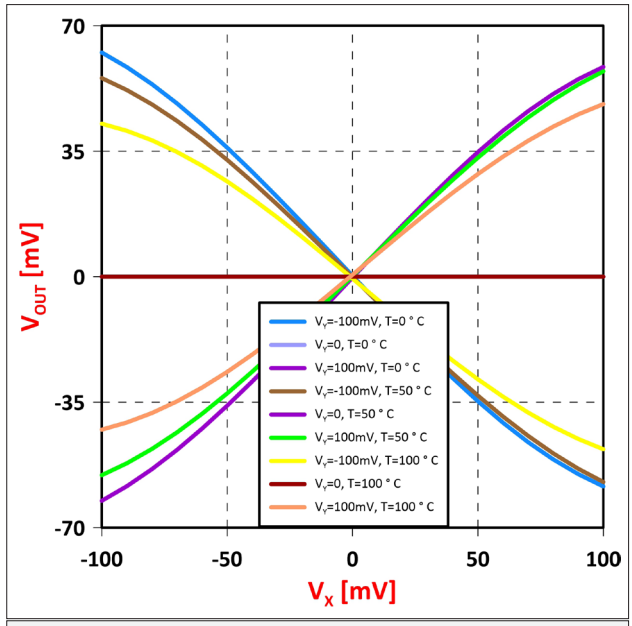

Figure 13. DC characteristics according to the temperature variation

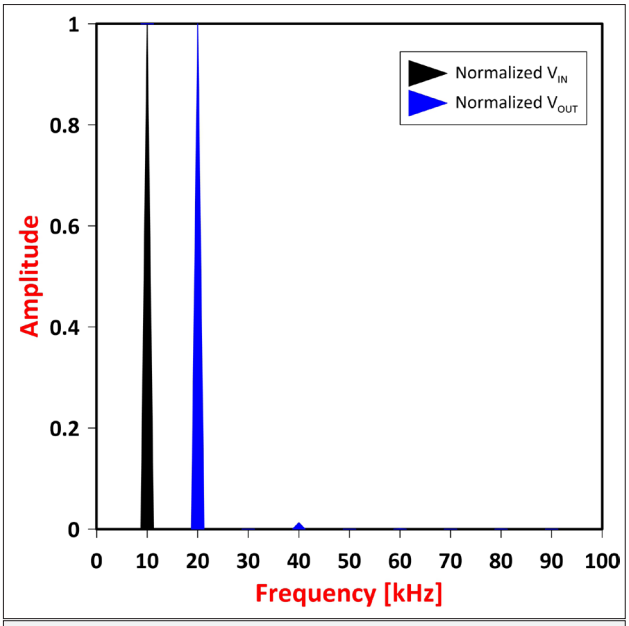

Figure 12. Frequency spectrum of the frequency doubler

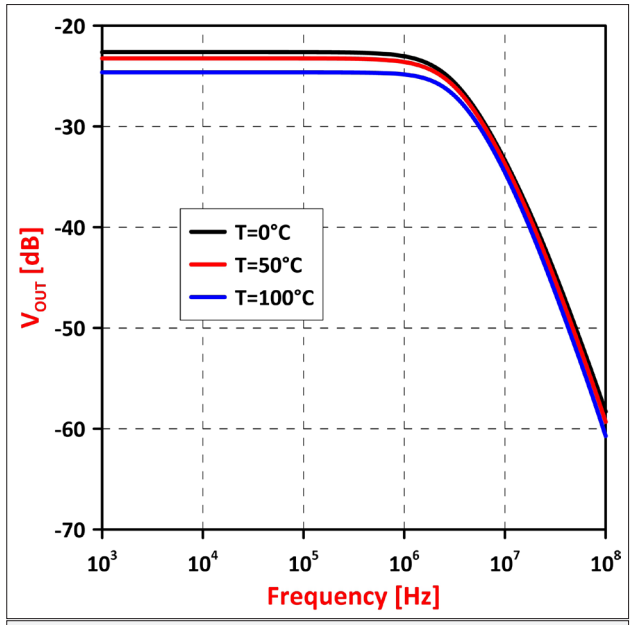

Figure 14. AC characteristics according to the temperature variation

Carlo analysis, a 10% change in process parameters and dimensions does not seem to affect the bandwidth value much.

Figure of Merit (FoM) is considered. *BW* is bandwidth (MHz), *InputRange* is input range (%), *THD* is total harmonic distortion (%) and *PC* is the power consumption (µW) of the circuit. The higher the FoM value, the better the circuit.

$$FoM = \frac{BW(MHz) \times InputRange(\%)}{THD(\%) \times PC(\mu W)} \quad (14)$$

The comparison of the proposed circuit and the studies in the literature is given in Table 3. Considering the FoM values, the low power consumption and linearity of the proposed FQAM stand out.

Conclusion

In this study, a DTMOS based four-quadrant analog multiplier is proposed. To evaluate the performance of the analog multiplier, the circuit has been tested in various applications such as amplitude modulator and frequency doubler. Intermodula-

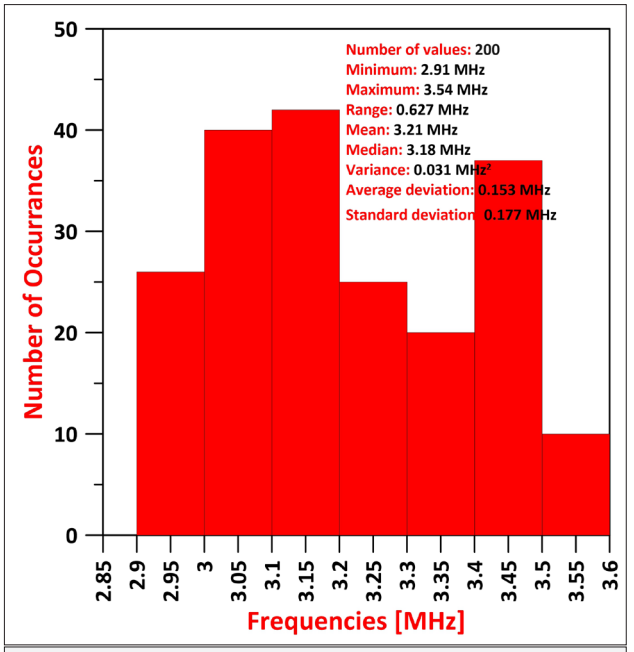

Figure 15. Bandwidth change obtained by changing the size (w) of MOS transistors by 10% of Monte Carlo analysis

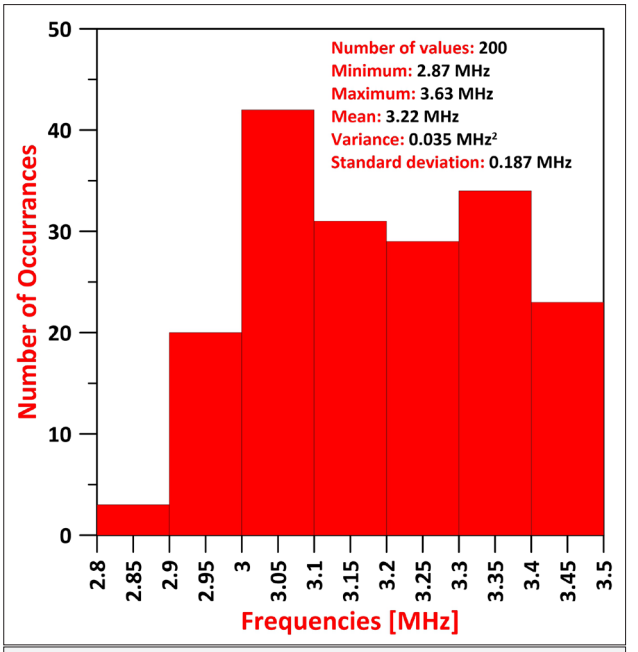

Figure 16. Bandwidth change obtained by changing the dimensions (W), VTH and tox parameters of MOS transistors of Monte Carlo analysis by 10%

Table 3. Comparison of previous studies and proposed FQAM circuit.

Ref	Year	Tech.	Power Supply	Bandwidth	THD	Power Consumption	Input Range	FoM
Ref	Year	Tech.	Power Supply	Bandwidth	THD	Power Consumption	Input Range	FoM
[30]	2006	0.35 µm	±2.5 V	30 MHz	0.62%	1.2 mW	±400 mV	32.26
[1]	2010	0.35 µm	1.5 V	268 kHz	4.2%	6.7 µW	±120 mV	2.29
[14]	2013	0.18 µm	0.5 V	221 kHz	5.8%	714 nW	±80 mV	8.54
[16]	2019	0.18 µm	±0.2 V	1.11 MHz	3.7%	18.4 nW	±200 mV	652.17
[29]	2019	0.5 µm	3.3 V	50 MHz	1%	660 µW	±200 mV	30.30
Proposed	-	45 nm	±0.2 V	3.23 MHz	1.2%	37 nW	±100 mV	14549.55

THD: Total Harmonic Distortion; FoM: Figure of Merit

tion products are calculated to show the effectiveness of the circuit when used as an amplitude modulator. Monte Carlo analysis was carried out to show its reliability against changes in the size of the circuit and process parameters. In Monte Carlo analysis, W, V_{TH} and tox parameters changed by 10%, but the average bandwidth remained the same. The highlights of the circuit are low supply voltage (±0.2 V), low power consumption (37 nW), bandwidth (3.23 MHz) and low THD (1.2%, full-scale input), input voltage range (±100 mV). Finally, FoM values are given to demonstrate the superiority of the proposed circuit over the studies in the literature.

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