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Warpage Reduction for Power MOSFET Wafers

Kim Ho Yeap[1], Humaira Nisar[1], Veerendra Dakulagi[2]

[1]Faculty of Engineering and Green Technology, Universiti Tunku Abdul Rahman, Kampar, Malaysia
[2]Department of Electronics and Communication Engineering, Guru Nanak Dev Engineering College, Karnataka, India

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ABSTRACT

Wafer warpage is a baseline issue faced by semiconductor manufacturers and is, in fact, particularly conspicuous among those which are involved in the fabrication of power metal oxide semiconductor field effect transistors (MOSFETs). This is because vertical MOSFETs experience larger warpage effects compared with their conventional lateral counterparts. Wafers with warpage exceeding its critical value fail to be chucked by vacuum adsorption during the automatic handling process; the devices fabricated in the wafer face reliability issues as well. This paper presents an analysis on various mechanisms employed to reduce warpage in power MOSFET wafers. The warpage behavior was examined by varying the backside metallization (BSM) thickness, the sputtering power for film deposition and the wafer's temperature (i.e., a cryogenic condition was introduced into the process). The results suggest that both the BSM thickness and wafer's temperature do not manifest a clear correlation with the wafer warpage when the front-end fabrication process is completed. The wafer bow level was, however, found to be in direct proportion with the magnitude of the sputtering power. When the sputtering power is reduced, less residual stress is induced to deform the wafer structure. Hence, the sputtering power could be adjusted to ensure that the warpage effect stays below its critical value.

Keywords: Warpage, power MOSFET, residual stress, backside metallization, sputtering power, cryogenic temperature

Corresponding Author:
Kim Ho Yeap

E-mail:
yeapkh@utar.edu.my;
yeapkimho@gmail.com

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Introduction

Although planar metal oxide semiconductor field effect transistors (MOSFETs) [1-3] have been widely implemented in the electronics industry [4], they are not well suited for power applications [5-7]. Unlike its conventional lateral arrangement, a power MOSFET takes the form of a vertical trench, with a varying design structure, depending on its trench technologies and applications [5]. Figure 1 and Figure 2 depict two of the most widely used trench structures. As can be clearly seen from the figures, a vertical trench is used to isolate the gate terminal from the substrate. The former structure utilizes, respectively, a thin and thick gate oxide at the upper and lower portions of the trench, resulting in a gate with an extended field plate, whereas the latter segregates the field plate from the gate, with the field plate connected to the ground to reduce the gate-to-drain capacitance [5]. Despite being structurally different, the operational concept of all trench power MOSFETs is similar. When the transistor is switched on, the carriers flow from the source across the body into the epitaxial layer and finally to the substrate, which is in direct contact with the drain electrode. The breakdown voltage of the device is dictated by the epitaxial thickness and its doping concentration and its current rating by the channel width. Hence, the trench power MOSFET is capable of sustaining higher breakdown voltage and carry higher current compared with its planar counterpart [8-16].

Wafer warpage is the deformation of the wafer structure into a saddle shape when stress is introduced to it during the fabrication process. This phenomenon is a consequence of the thermal expansion coefficient (CTE) mismatch among different stacked materials deposited onto the wafer. As the temperature cools down, the films and the substrate contract at different rates. The wafer, therefore, warps upward or downward to accommodate the residual stress induced within [17]. Owing to the presence of the vertical trenches, power MOSFET wafers are more susceptible to the warpage effect in comparison with the planar MOSFET wafers. As a

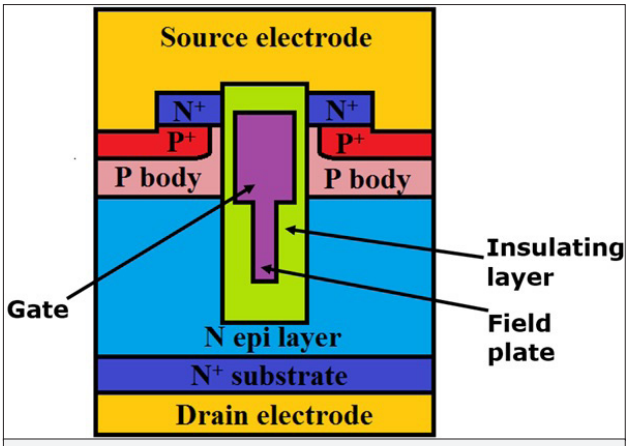

Figure 1. A terraced oxide field plate trench power MOSFET

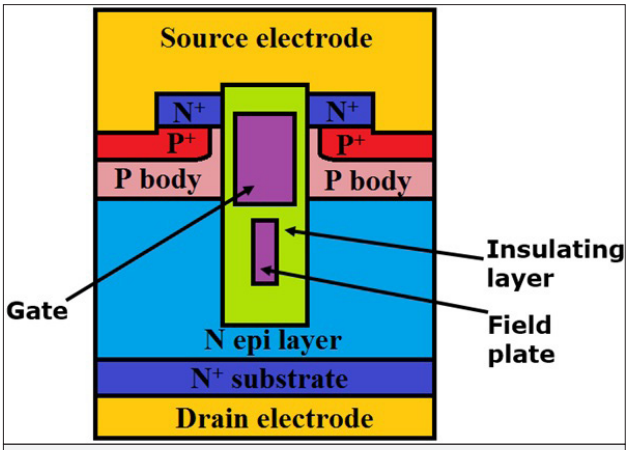

Figure 2. A split-gate trench power MOSFET

matter of fact, power MOSFETs with the same mesa width are observed to sustain higher level of warpage effect when the depth of the trench increases.

Warpage is a serious baseline issue in the semiconductor manufacturing industry It may result in failure in the photolithography, wafer sawing, and chip packaging processes [18-20]. It may also impose reliability issue on the devices fabricated in the wafer [21-25]. In fact, wafers with warpages exceeding the permissible limit fail to be chucked by vacuum adsorption during the automatic handling process [9, 10] and are, therefore, hampered from proceeding to the subsequent fabrication steps.

Throughout the years, attempts have been made to curb warpage effects that occur at the front end (FE) [8-10, 25-27] and back end (BE) [18, 28] manufacturing lines. The formation of warpages at the FE line is perceived to be particularly critical. If appropriate actions to contain the warpages at the FE stage are not taken, the effect may propagate and its level of severity would exacerbate at the BE stage. Here, we investigate the methods that could be implemented at the FE to minimize the warpage effect.

Methods to reduce warpage effects for power MOSFET wafers at the FE line are surprisingly rare in the literature. Among them are the methods proposed by Zhang et al. [8] and Kato et al. [9, 10]. The methods formerly emphasize on the process of film depositions, whereas those proposed later emphasize on the process of transistor fabrication. Comparisons of the conditions before and after the implementation of the process control techniques were not clearly shown. Furthermore, modifications on the backside metallization (BSM) films and the introduction of cryogenic temperature were not included in their methods. Although the works in [25] and [26] proposed, respectively, the variation of the wafer's temperature (i.e., cryogenic environment is introduced into the manufacturing process) and the sputtering power for BSM film deposition, the experiments were carried out in generic wafers, which were not designed specifically for power MOSFETs. Hence, they may not be able to provide an accurate insight into the warpage behavior for these wafers. Furthermore, the factors were analyzed separately within a stipulated range of boundary conditions (such as the types of films used, the manufacturing procedure, etc.). However, in reality, these factors are integrated as a whole and may have intertwining influence on each other. In this paper, we re-examine the impact of these 2 factors on the warpage behavior in trench power MOSFET wafers. As discussed in the following section, the warpage effect is only found to be pronounced at the end of the FE process. Hence, the adjustment of the passivation layer (which lies in the middle of the process), as proposed by [28, 29], is omitted in our case study here. Instead, we investigated the final step of the FE process; we varied the BSM thickness and observed its effect on warpage behavior. To present a thorough analysis, we measured the warpage effect only when the fabrication process is completed at the FE manufacturing line.

Bow Measurements

The warpage effect is estimated based on the bow level of the wafers. The degree of curvature of the bow is measured using the ISIS tool via optical sensing. Figure 3 depicts the structure of the tool. As can be seen from the figure, a circular plate is used to hold the wafer at the bottom and an optical sensor is placed perpendicularly above it. In the measurement process, 8-inch trench power MOSFET wafers with a thickness of 725 µm were used. As wafer bow may be affected by the trench depth, number of metal stacks, and number of BSM layers, these variables were kept constant throughout the process. The depth of the trench was set approximately at 6.3 µm and each wafer consisted of 3 BSM layers (Ti, NiV, and Ag), AlSiCu metal stacks, and a layer of polyimide passivation. To ensure accuracy in the measurement process, the bow level for each wafer was taken twice and the average was recorded. To minimize the number of uncertainties, the wafers were fabricated at the same timeframe, using identical tools and chambers. The chemicals used during the cleaning and etching processes comprised the same lifetime as well.

As mentioned in the preceding section, 3 parameters were varied to investigate their impacts on the warpage behavior,

namely, the BSM thickness, the sputtering power, and the wafer's temperature. When varying the parameter of 1 factor, those for the other 2 were kept constant. The wafer with 200 nm, 500 nm, 200 nm, 5 µm, and 6 µm thicknesses for the Ti, NiV, Ag, AlSiCu, and polyimide films, respectively, 2.38 mm bow level, and sputtering power fixed at 5 kW was used as the point of reference for the three experiments.

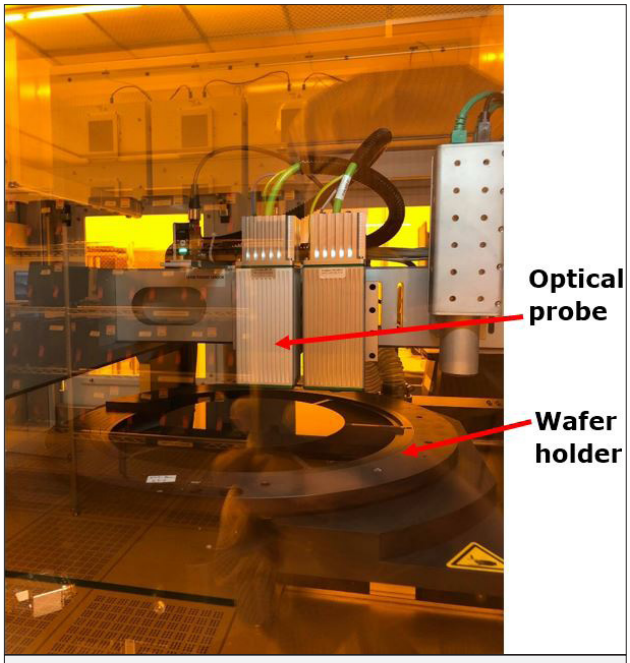

Figure 3. The ISIS tool used for wafer warpage measurements

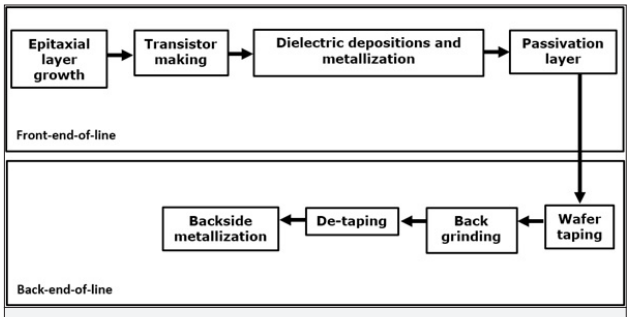

Figure 4. Front-end trench power MOSFETs manufacturing process flow

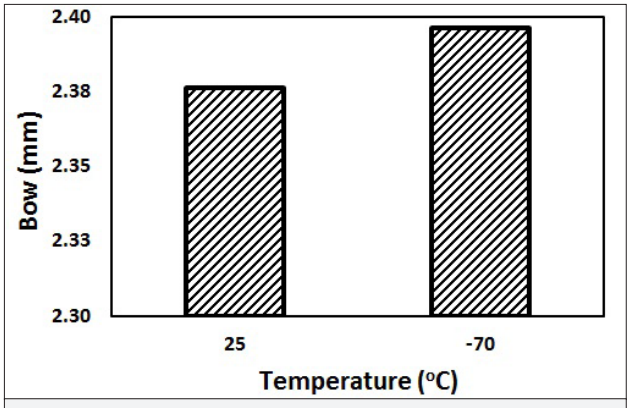

Figure 5. The bow levels of power MOSFET wafers with and without undergoing cryogenic condition

Fabrication Process

The block diagram in Figure 4 summarizes the fabrication process of the power MOSFET wafer. In general, the FE process consists of 2 sections, i.e., the front-end-of-line (FEOL) and the back-end-of-line (BEOL). The FEOL includes the fabrication of the power MOSFET transistors and the metal interconnections to form circuitries, whereas the BEOL constitutes the deposition of the BSM, which is necessary in power MOSFETs to provide ohmic contact to the wafer, to prevent diffusion of metals to the electrode, and to allow the die to be soldered onto the lead frames [5].

The fabrication begins with the growth of an n-type (either phosphorous or arsenic) epitaxial layer onto the substrate. A diffused p-type boron body and a shallower n+ diffused source are then formed within the epitaxial drain [5]. A narrow trench is subsequently etched and an oxide layer is grown within it. The transistor making process is completed when the phosphorous-doped polysilicon gate fills the trench via chemical vapor deposition. To interconnect the transistors, the wafer surface is to be initially filled with dielectric materials. The first layer of dielectric is known as the pre-metal dielectric (PMD), whereas the subsequent layers are inter-metal dielectric (IMD). Before each inter-layer dielectric is deposited, it is etched and filled with Tungsten vias. Metallization is then formed by depositing AlSiCu metal stacks onto the dielectric layers [30, 31]. Finally, polyimide is deposited at the top of the wafer as the passivation layer.

As soon as the passivation layer is completed, the wafer is sent to the BEOL for backside grinding. The purpose of doing so is to reduce the overall thickness of the chip. However, before the wafer is thinned, the front side of the wafer has to be taped so as to

protect the chip from contaminants and mechanical abrasion. At the final stage, the tape is removed and BSM is deposited onto the surface of the wafer. Once the process is finished, the wafer is transferred to the BE manufacturing line for dicing, sorting, and lastly, packaging.

Results

Figures 5-7 summarize the results attained from the three experiments. In the first experiment, an additional step of cooling down the wafer to cryogenic temperature for 60 minutes using liquid nitrogen (-70°C) was introduced. This step was conducted after the passivation process and before the back-grinding tape was applied onto the wafer surface. As can be seen in Figure 4, this process was performed at the final phase of the FEOL, i.e., before BSM layers were deposited. Figure 5 illustrates the bow levels of the wafers with and without this additional step. According to Cheng et al. in [25], wafer warpages will

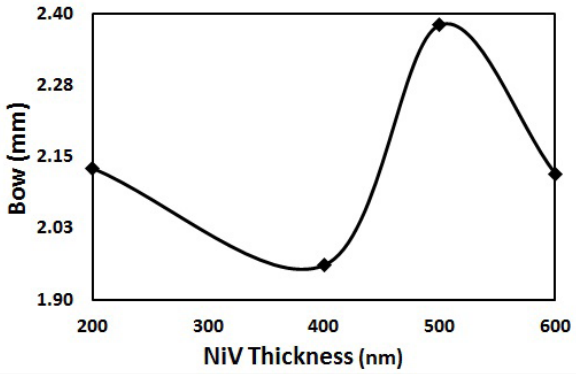

Figure 6. The bow level of power MOSFET wafers when NiV thickness is varied

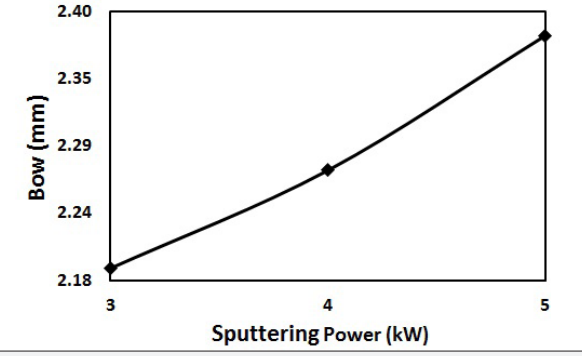

Figure 7. The bow level of power MOSFET wafers when the NiV sputtering power is varied

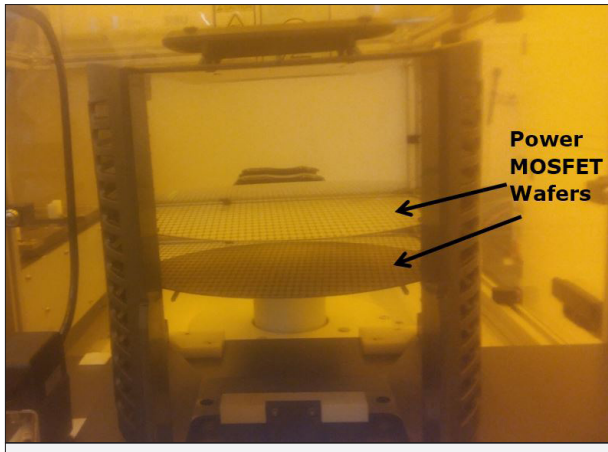

Figure 8. Two trench power MOSFET wafers with different warpages

be reduced when the operating temperature reverted from extremely low to ambient temperature. It is interesting to see, however, from Figure 5 that the bow levels of the two wafers are comparable; the deviation is only approximately 0.02 mm. As the bow level was only measured after the entire FE manufacturing process is completed, the result suggests strongly that the warpage effect may only occur after the deposition of the BSM layers.

Table 1. Thermal expansion coefficients of the conducting materials used in backside metallization

Material	CTE at 20°C ($\times 10^{-6}$ K^{-1})
Silver (Ag)	18.0
Nickel (Ni)	13.0
Titanium (Ti)	8.6
Vanadium (V)	8.4

In the second experiment, the NiV thickness of the BSM was varied. The Pearson correlation coefficient r can be calculated using (1) below:

$$r = \frac{n\sum_{i=1}^{n} x_i y_i - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} y_i}{\sqrt{\left[n\sum_{i=1}^{n} x_i^2 - \left(\sum_{i=1}^{n} x_i\right)^2\right]\left[n\sum_{i=1}^{n} y_i^2 - \left(\sum_{i=1}^{n} y_i\right)^2\right]}} \quad (1)$$

where n=4 is the total number of samples, x_i and y_i are, respectively, the ith number of the NiV thickness and the bow level. By substituting the experimental data in Figure 6 into (1), r was found to be as low as 0.2391. This is to say that the bow level does not register a distinctive correlation with the NiV thickness. The NiV layer was sandwiched between the Ag and Ti, BSM layers and the CTEs of the materials are tabulated in Table 1. At any temperature T, the thermal stress σ_T is proportional to [32]:

$$\sigma_T \propto (T_{dep} - T)\Delta\alpha \quad (2)$$

where T_{dep} is the deposition temperature and Δα is the difference between the CTE of the two adjacent materials. As the CTEs of nickel and vanadium are, respectively, close to that of silver and titanium, Δα is small. As a result, the thermal stress induced at the BSM layers is small as well. This shows that the NiV layer serves as an effective stress buffer for the other two conducting layers. Hence, the variation of its thickness may not directly contribute to the intrinsic stress induced at the BSM layers.

The third experiment was conducted when the first and second did not render any conclusive results. In the third experiment, the sputtering power for depositing the NiV film was varied from 3 kW to 5 kW. As shown in Figure 7, the bow level increases linearly with the supplied power. The result is in contrast with the finding in [26], which shows that the warpage effect improves with increasing sputtering power. It is to be noted, however, that the work in [26] is based on the variation of RF power between 100 W and 300 W and it is used to sputter Mo on Mo/Si multilayer films. Unlike the Mo film, which exhibits tensile stress at the upper layer [26], the NiV film deposited here relieves the intrinsic stress (i.e., it acts as a buffer) experienced by the Ag and Ti films at the bottom of the wafer. Hence, it may not be adequate to perform a direct comparison between these two works. It is, nevertheless, appropriate to conclude at this point that less residual stress would be induced to deform the wafer structure if the NiV sputtering power is curtailed. Figure 8 illustrates two power MOSFET wafers treated using different

sputtering powers. The NiV layer at the top wafer is sputtered using higher RF power compared with the one at the bottom. It is apparent from the figure that the warpage effect at the top wafer is more severe than that at the bottom. Upon close inspection of the top wafer, it can be observed that the warpage condition is irregular in that the wafer warps positively upward at both edges, with the left side warps relatively higher than the right side. This suggests that the stress is non-uniformly distributed throughout the wafer.

Conclusion

In this paper, 3 different mechanisms had been conducted to reduce warpages in power MOSFET wafers: (1) cryogenic temperature was introduced into the fabrication process and (2) the NiV thickness of the BSM and (3) its sputtering power were varied. As a direct correlation between the first and second mechanisms with the warpage behavior could not be found, it may not be practical to apply them in the wafer manufacturing process. The NiV sputtering power, in contrast, is found to be directly proportional to the warpage effect. Hence, it could be adjusted so that the bow level is kept below its permissible limit.

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Conflict of Interest: The authors have no conflicts of interest to declare.

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Kim Ho Yeap received his BEng (Hons) from Universiti Teknologi Petronas in 2004, MSc from Universiti Kebangsaan, Malaysia in 2005, and PhD from Universiti Tunku Abdul Rahman in 2011. In 2008 and 2015, he was a visiting researcher at University of Oxford and Nippon Institute of Technology, respectively. Yeap is a senior member of the IEEE and a member of the IET. He is also a Chartered Engineer registered with the UK Engineering Council and a Professional Engineer registered with the Board of Engineers Malaysia. He is currently an Associate Professor in Universiti Tunku Abdul Rahman. Throughout his career, Yeap has served in various administrative capacities, including the Head of Programme of Master of Engineering Science and the Head of Department of Electronic Engineering. Yeap's areas of interests are radio astronomy, electromagnetics, and microelectronics. He has published 74 journal papers, 39 conference proceedings, 7 books, and 13 book chapters. Yeap is the external examiner of Wawasan Open University. He is the Editor-in-Chief of the i-manager's Journal on Digital Signal Processing. Yeap has been given various awards, including the university teaching excellence award, 4 Kudos awards from Intel Microelectronics, and 19 research grants.

Humaira Nisar has a B.S (Honours) in Electrical Engineering from University of Engineering and Technology, Lahore, Pakistan; M.S in Nuclear Engineering from Quaid-i-Azam University, Islamabad, Pakistan; and another M.S in Mechatronics and Ph.D in Information and Mechatronics from Gwangju Institute of Science and Technology, Gwangju, South Korea. She has more than twenty years of research experience. Currently she is working as an Associate Professor in the Department of Electronic Engineering, Universiti Tunku Abdul Rahman, Malaysia. She worked as the Head of Master of Engineering Science Programme for five years. Currently, she is the Head Master of Engineering (Electronic Systems) programme. She is a senior member of IEEE. Her research interests include signal and image processing, biomedical imaging, brain signal and image analysis, and image analysis for wastewater treatment. She has published more than 150 international journal and conference papers.

Veerendra Dakulagi earned his B.E. in electronics and communication engineering (E&CE) and M.Tech. in power electronics from Visvesvaraya Technological University, Belagavi, India, in 2007 and 2011, respectively. He earned his Ph.D. degree in array signal processing from the same university in 2018. He worked as a lecturer in Sapthagiri Engineering College, Bangalore, India, from 2007 to 2008. Then, he worked as Assistant Professor in Bheemanna Khandre Institute of Technology, Bhalki, India, from 2009 to 2010. He worked as Assistant Professor in department of E&CE, Guru Nanak Dev Engineering College, Bidar, India, from 2010 to 2018. Currently, he is Dean (Research & Development) and Associate Professor (E&CE) of the same institute. He has published over 30 refereed technical journals (including IEEE Transactions, IEEE Journals, Elsevier, Springer, and Taylor & Francis) and 1 patent in array signal processing. He has received many awards in education, including (1) the 'Award for Research Publications' by vision group on science and technology, Govt. of Karnataka, India under the leadership of Bharat Ratna Prof. C.N.R. Rao and (2) the Best teacher/researcher award by Guru Nanak Dev Engineering College, Bidar, for the academic year 2018–19. He is the Editor-in-Chief of the (1) Journal of Advanced Research in Wireless, Mobile & Telecommunication and (2) Journal of Advanced Research in Signal Processing & Applications. Also, he serves as an Associate Editor for the following Journals: (1) Communication Engineering and Systems and (2) Journal on Electronics Engineering. He is a regular reviewer to various IEEE transactions/journals, Elsevier, Taylor & Francis, and Springer journals.