

Analysis of a Modified Switching Pattern for Packed U Cell-15 Inverter Topology with Advanced Level Shift Carrier Pulse Width Modulation Techniques

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ABSTRACT

This paper focused on the design and analysis of a modified switching sequence for a 15-level Packed U Cell (PUC-15) inverter. The proposed switching sequence improved the harmonic spectrum, reduced the burden on switches, and controlled the switching frequency. The performance of the inverter was also observed in terms of total harmonic distortion (THD) with constant frequency (phase disposition [PD] and phase opposition disposition [POD]) and variable frequency, variable frequency carrier opposition (VFCO) level shift triangular carrier-based sinusoidal pulse width modulation (SPWM) techniques at different modulation indices of $M = 0.2, 0.4, 0.6, 0.8$, and 1. Insights from the modified switching sequence and pulse width modulation techniques were analyzed and compared via simulations in a MATLAB/Simulink environment. By analyzing the results, it showed that the PD-PWM technique produced better results than other modulation techniques, and that the voltage and current THD% obtained therefrom 2.49% and 1.86% at $M = 1$, which comes under IEEE-519 standard.

Keywords: Multilevel inverter, packed U cell, phase disposition, phase opposition disposition, variable frequency, variable frequency carrier opposition, total harmonic distortion

Research Motivation

Power industries currently use inverters to convert power from one state of level into another. In power conversions, advanced multilevel inverters (MLI) influence various features as follows:

1. Lowering harmonic distortion
2. Using fewer switches with more levels
3. Staircasing outputs
4. Performing regulatory functions with fundamental, medium, and higher frequencies
5. Minimizing switching losses
6. Providing transient electromagnetic interference (EMI) capability and high-quality power outputs

This study incorporated these features by modifying the existing control switching sequence for a packed U cell 15 (PUC-15) MLI. This modified switching sequence helped maintain harmonics results under IEEE-519 standard.

Literature Review

MLIs are highly reliable components used in power semiconductor devices to convert power and compensate reactive power. MLIs are pre-owned to work effectively at high-power high-voltage and neutral-power neutral-voltage applications with an MLI strategic control structure of [1, 2]. Basic conventional MLIs are used to overcome the problems in 2-level multilevel inverters, which have high-order harmonics and are partially controlled using large capacitive filters. The first conventional MLIs were neutral-point clamped (NPC) inverters proposed by Nabae in 1981 [3] to overcome power electronic component stress, but this topology had several technical complications for higher-frequency operations and needed more clamping diodes level by level. Another conventional MLI by Meynard et al. [4] proposed fiber channel (FC) topology using capacitors, but these are uneconomical compared with diodes and have

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voltage balance problems across capacitors. Another conventional MLI by Mariusz Malinowski et al. [5] cascaded H-bridge (CHB) topology that required separate DC sources for each module and had increasing levels of complexity in operation, cost, and EMI. Therefore, researchers are working on modified and advanced multilevel inverter configurations like Packed U Cell [6-12], T-type [13], nested [14], and cross-switched T-type (CT-Type) [15]. This study provides insights into the recently introduced PUC MLI [16, 17].

We have identified that asymmetrical MLIs help control higher harmonic levels and develop transient output waveforms compared with symmetrical MLIs. Switching pressures at asymmetric MLIs are varied and low; however, symmetrical MLIs work the same with higher switching pressures for power semiconductor components. Moreover, asymmetrical MLIs have lower PSCs, lower switching pressure with higher output voltage levels, and lower order harmonics. The topology of the PUC has fewer switches with reduced device count of power components. Therefore, its overall efficiency increases with low stress on power switches, preventing the need for bulky installations because its transformer requires less construction. The main applications are power generation systems, industrial drives, and power quality improvements. Table 1 compares semiconductor components for different traditional multilevel inverters and 15-PUC MLI.

In reviewing the literature, we found that some 15-level inverters do not show perfect 15-level output voltages and show high harmonics [18-21]. The existing 15-level PUC inverters show uneven 15-level output voltages because of the usage of conventional switching sequences. Therefore, researchers are focusing on this problem to control harmonics at 15-level output voltages (above 0 at 7 levels, below 0 at 7 levels and the central level) with a modified switching sequence. The PUC MLIs are controlled using different constants and variable switching frequency pulse width modulation (PWM) controllers at different modulation indices (MI). Figure 1 shows the modulation methods for MLI topologies.

Contributions of This Study

- A modified switching sequence is proposed for PUC-15 to replace a conventional switching sequence for controlling switching pressures with lower harmonics.

Table 1. Semiconductor components for 15-level inverters

Name	NPC	FC	CHB	HCHB	PUC
Switches	28	28	28	12	08
Diodes	26	0	0	0	0
DC bus capacitors	14	14	07	03	03
Total components	68	42	35	15	11

FC: flying capacitor; CHB: cascaded H-bridge; PUC: packed U cell; NPC: neutral-point clamped; HCHB: hybridized cascaded H-bridge

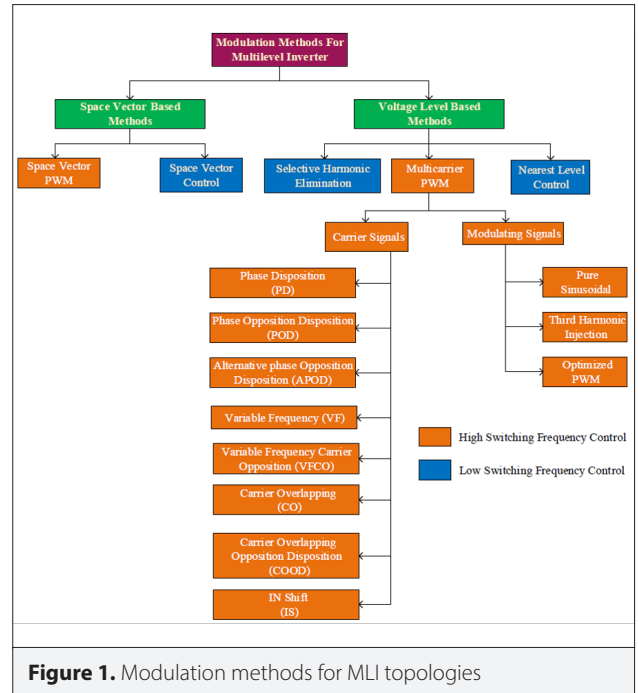


Figure 1. Modulation methods for MLI topologies

- To control the PUC-15 MLI constant switching frequency carrier-based PWM method, phase disposition (PD) and phase opposition disposition (POD) techniques are analyzed at different MI of 0.2, 0.4, 0.6, 0.8, and 1.0.
- To control the PUC-15 variable switching frequency, a carrier-based PWM method is also analyzed with variable frequency (VF) and variable frequency carrier opposition (VFCO) techniques at different MI of 0.2, 0.4, 0.6, 0.8, and 1.0.
- The performance of the modified switching sequence is analyzed and compared with the different PWM techniques at multiple modulation indexes and represented graphically.

In this article, we discuss mainly the following:

- Section I: Design and analysis of PUC-15 topology
- Section II: PWM techniques
- Section III: Simulation and theoretical result analysis
- Section IV: Performance analysis
- Sections V, VI, and VII: Conclusion, references, and nomenclature.

Designing and Analysis of PUC-15 Topology

A basic PUC is shown in Figure 2; it consists of 1 voltage source and 2 power switches. This basic PUC generates 3 output voltage levels: +V, 0 and -V. According to the basic PUC structure, 15-level output voltage is developed using three cascaded PUCs. The basic PUC has small power devices for high-quality energy conversions and lower production costs, Figure 3 represents single phase PUC-15 inverter.

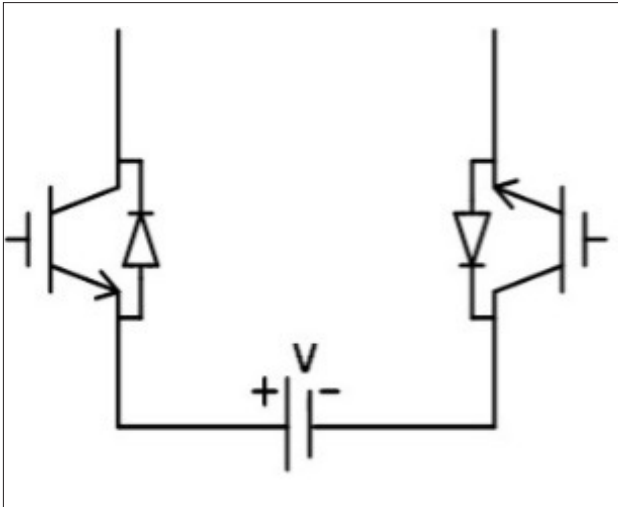


Figure 2. Initial model of packed U cell

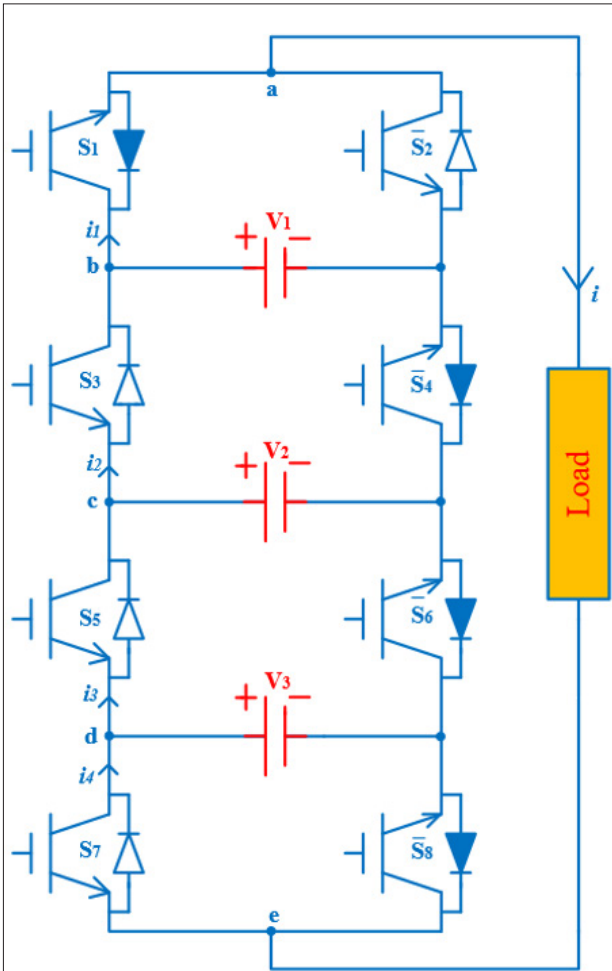


Figure 3. Single phase PUC-15 MLI

Generalized expressions of the number of levels are represented by the equations (1) and (2) [3].

Table 2. Modified switching sequence for PUC-15 MLI

Mode	S_1	S_3	S_5	S_7	Level
1	1	0	0	0	$7V (V_1)$
2	1	0	0	1	$6V (V_1-V_3)$
3	1	0	1	0	$5V (V_1-V_2+V_3)$
4	1	0	1	1	$4V (V_1-V_2)$
5	1	1	0	0	$3V (V_2)$
6	1	1	0	1	$2V (V_2-V_3)$
7	1	1	1	0	$1V (V_3)$
8	0	0	0	0	$0V$
9	0	0	0	1	$-1V (-V_3)$
10	0	0	1	0	$-2V (V_3-V_2)$
11	0	0	1	1	$-3V (-V_2)$
12	0	1	0	0	$-4V (V_2-V_1)$
13	0	1	0	1	$-5V (V_2-(V_1+V_3))$
14	0	1	1	0	$-6V (V_3-V_1)$
15	0	1	1	1	$-7V (-V_1)$

PUC-15: packed U cell 15 level; MLI: multilevel inverter

$$N \text{ (number of organized levels)} = 2^{n+1} - 1 \quad (\text{where } n = 1, 2, 3, \dots)$$

The number of switches required, N_{sw} depend on the quantity of generation voltage levels N . A generalized expression of N_{sw} is given by following equation:

$$N = 2^{\frac{N_{sw}}{2}} - 1 \quad 2$$

The modified switching sequence of PUC-15 MLI is shown in Table 2. This table represents 8 switches (S_1 to S_8) only at the 15 level; and these switches (S_1 and S_2), (S_3 and S_4), (S_5 and S_6) and (S_7 and S_8) act in a complimentary manner; this means that they operate in opposition, at different time periods, and independently. The modified switching sequence of the 15-level PUC MLI operates mainly 15 operating voltage level modes; for a positive half-cycle, the voltage levels are $7V (V_1)$, $6V (V_1-V_3)$, $5V (V_1-V_2+V_3)$, $4V (V_1-V_2)$, $3V (V_2)$, $2V (V_2-V_3)$, $1V (V_3)$, $0V$, $-1V (-V_3)$, $-2V (V_3-V_2)$, $-3V (-V_2)$, $-4V (V_2-V_1)$, $-5V (V_2-(V_1+V_3))$, $-6V (V_3-V_1)$, $-7V (-V_1)$. Central mode, which considers all ones or zeros and DC source voltage levels balanced equations, is accomplished by

$$\frac{V_1}{V_2} = \frac{7}{3}, \frac{V_2}{V_3} = 3 \quad 3$$

$V_1=230V, V_2=99V, V_3=33V$ are the voltages.

Table 3 represents the conventional switching sequence of a 15-level PUC MLI [6, 7, 17]. Tables 2 and 3 show that for, the switching sequences are quite different; the voltage combinations of modes ((2-3) and (13-14)) are also different, with different switching sequences for particular levels. Moreover, mode 8 is the complete opposite of the conventional switching sequence.

From Figure 3, the node voltage equation is [3, 6, 10, and 11]

Table 3. Conventional switching sequence for PUC-15 MLI

Level & Mode	S_1	S_3	S_5	S_7	DC voltage combination
1	1	0	0	0	7V (V_1)
2	1	0	1	0	6V ($V_1 - V_2 + V_3$)
3	1	0	0	1	5V ($V_1 - V_3$)
4	1	0	1	1	4V ($V_1 - V_2$)
5	1	1	0	0	3V (V_2)
6	1	1	0	1	2V ($V_2 - V_3$)
7	1	1	1	0	1V (V_3)
8	1	1	1	1	0V
9	0	0	0	1	-1V ($-V_3$)
10	0	0	1	0	-2V ($V_3 - V_2$)
11	0	0	1	1	-3V ($-V_2$)
12	0	1	0	0	-4V ($V_2 - V_1$)
13	0	1	1	0	-5V ($V_3 - V_1$)
14	0	1	0	1	-6V ($V_2 - (V_3 + V_1)$)
15	0	1	1	1	-7V ($-V_1$)

$$V_{ae} = V_{ab} + V_{bc} + V_{cd} + V_{de} \quad 4$$

Equation (4) represents four node voltages (a, b, c, d) each, and every node voltage is as concise as follows:

$$\begin{cases} V_{ab} = (S_1 - 1)V_1 \\ V_{bc} = (1 - S_3)(V_1 - V_2) \\ V_{cd} = (1 - S_5)(V_2 - V_3) \\ V_{de} = (1 - S_7)V_3 \end{cases} \quad 5$$

Using eq. (5) in eq. (4),

$$\begin{aligned} V_{ae} &= (S_1 - 1)V_1 + (1 - S_3)(V_1 - V_2) + (V_2 - V_3)(1 - S_5) + (1 - S_7)V_3 \\ V_{ae} &= S_1V_1 - V_1 + V_1 - V_2 - S_3V_1 + S_3V_2 + V_2 - V_3 - S_5V_2 + S_5V_3 + V_3 - S_7V_3 \\ V_{ae} &= (S_1 - S_3)V_1 + (S_3 - S_5)V_2 + (S_5 - S_7)V_3 \end{aligned} \quad 6$$

From Figure 3, the current equations at the node b, c, and d are:

$$\begin{cases} i_1 = S_1i_l \\ i_2 = S_3i_l \\ i_3 = S_5i_l \\ i_4 = S_7i_l \end{cases} \quad 7$$

Applying Kirchhoff's current law at node b, we obtain the following:

$$\begin{aligned} i_1 &= i_2 + i_{c1} + i_l \\ i_{c1} &= i_1 - i_2 - i_l \\ \frac{dV_1}{dt} &= \frac{(S_1 - S_3)}{C} i_l = \frac{i_l}{C} S_1 - \frac{i_l}{C} S_3 \end{aligned} \quad 8$$

Applying Kirchhoff's voltage law at node c, we get:

$$\begin{aligned} i_2 &= i_3 + i_{c2} + i_l \\ i_{c2} &= i_2 - i_3 - i_l \\ \frac{dV_2}{dt} &= \frac{(S_3 - S_5)}{C} i_l = \frac{i_l}{C} S_3 - \frac{i_l}{C} S_5 \end{aligned} \quad 9$$

Applying KCL at node d, we obtain:

$$\begin{aligned} i_3 &= i_4 + i_{c3} + i_l \\ i_{c3} &= i_3 - i_4 - i_l \\ \frac{dV_3}{dt} &= \frac{(S_5 - S_7)}{C} i_l = \frac{i_l}{C} S_5 - \frac{i_l}{C} S_7 \end{aligned} \quad 10$$

Applying KVL at load, we get:

$$V_l = V_{ae} - i_l R_l - L_l \frac{di_l}{dt} \quad 11$$

Equation (9) can be rewritten as follows:

$$\begin{aligned} \frac{di_l}{dt} &= -\frac{V_l}{L_l} + \frac{V_{ae}}{L_l} - \frac{i_l R_l}{L_l} \\ \frac{di_l}{dt} &= \frac{(S_1 - S_3)}{L_l} V_1 + \frac{(S_3 - S_5)}{L_l} V_2 + \frac{(S_5 - S_7)}{L_l} V_3 - \frac{V_l}{L_l} - \frac{i_l R_l}{L_l} \\ \frac{di_l}{dt} &= \frac{S_1 V_1}{L_l} - \frac{S_3 V_1}{L_l} + \frac{S_3 V_2}{L_l} - \frac{S_5 V_2}{L_l} + \frac{S_5 V_3}{L_l} - \frac{S_7 V_3}{L_l} - \frac{V_l}{L_l} - \frac{i_l R_l}{L_l} \\ \frac{di_l}{dt} &= \frac{S_1 V_1}{L_l} + \frac{(V_2 - V_1)}{L_l} S_3 + \frac{(V_3 - V_2)}{L_l} S_5 - \frac{S_7 V_3}{L_l} - \frac{V_l}{L_l} - \frac{i_l R_l}{L_l} \end{aligned} \quad 12$$

According to models of the state space equation for non-linear systems according to time, varying PUC-15 MLI results in the following:

$$\dot{X} = A(x, t) \times x + B(x, t) \times u + c(t) \quad 13$$

From equation (11), if the parameters for 15-level PUC MLI ($X_1=i_1, V_1=X_2, V_2=X_3, V_3=X_4$) are assumed then the state space equations [3, 6, 10, 11] can be modeled as follows:

$$\begin{aligned} A(x, t) &= \begin{bmatrix} -R_l \\ L_l \\ 0 \end{bmatrix}, c(t) = \begin{bmatrix} -V_l \\ L_l \\ 0 \end{bmatrix}, u = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \end{bmatrix} \\ B(x, t) &= \begin{bmatrix} X_2 & X_3 - X_2 & X_4 - X_3 & -X_4 \\ L_l & L_l & L_l & L_l \\ 0 & 0 & -X_1 & X_1 \\ & & C & C \end{bmatrix} \end{aligned}$$

Pulse Width Modification Techniques

Multilevel inverters are usually controlled using various open- and closed-loop methods and algorithms [16]. In open-loop methods, PUC-15 MLI topology is controlled with different advanced triangular carrier-based SPWM techniques. The usage methods of carrier-based advanced SPWM techniques are described below.

The PUC-15 MLI considers 14 triangular multi-carrier only (number of carriers = number of levels - 1) shown in eq. (15); every triangular carrier has one maximum position at the mid-point of the carrier and two minimum positions at the start and stop positions of the carrier.

$$N_c = N_L - 1$$

where N_c = number of usage carriers and N_L = Number of output levels

Phase Disposition Triangular Based Multi-Carrier Sinusoidal Pulse Width Modulation Technique (PD-SPWM)

In PD-SPWM method, all 14 carriers are identical and operate on the same switching frequency, with the same amplitude and phase with equal displacements, as shown in Figure 4.

Phase Opposition Disposition Triangular based Multi-Carrier SPWM Technique (POD-SPWM)

In POD-SPWM method, all 14 carriers are not identical and operate on the same switching frequency with the same amplitude; positive and negative level amplitude carriers are placed with a phase shift between them, as shown in Figure 5.

Variable Frequency Triangular Carrier-based PWM Technique (VF-SPWM)

In VF-SPWM method, all 14 carriers are arranged along similar amplitudes and phases but the carriers developed vary for different frequencies, as shown in Figure 6.

VFCO Variable Frequency Triangular Carrier-based PWM Technique (VF-SPWM)

In the VFCO-SPWM method, all 14 carriers are arranged along the same amplitude, negative amplitude level carriers are phase to positive amplitude carriers, and carriers for different frequencies vary, as shown in Figure 7.

Analysis of Simulation and Theoretical Results

The simulations of PUC-15 MLI were carried out using triangular carrier-based advanced SPWM techniques with constant and variable frequencies (PD, phase opposition disposition

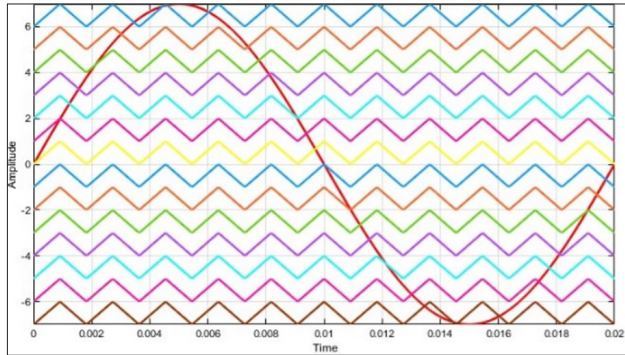


Figure 4. Triangular based multi-carrier PD-SPWM

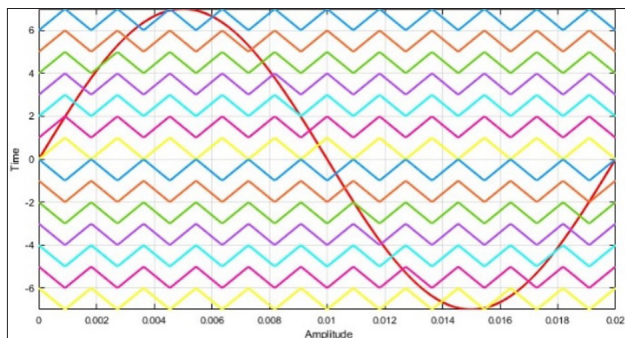


Figure 5. Triangular based multi-carrier POD-SPWM

(POD), VF, and VFCO). Table 4 shows the electrical parameters, Figure 8 shows the simulation model of PUC-15 MLI, and Figure 9 represents the triangular multi-carrier sinewave with 15-level output voltage. PUC-15 level compared sinewave and triangular carriers using a modified switching sequence, with dotted lines representing particular stepwise voltage level indications.

Figure 10 represents the required switching pulses for PUC-15 MLI. These pulses are highly impactful to develop perfect PUC-

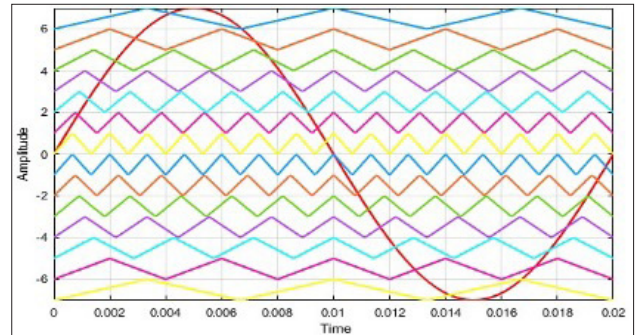


Figure 6. Triangular based multi-carrier VF-SPWM

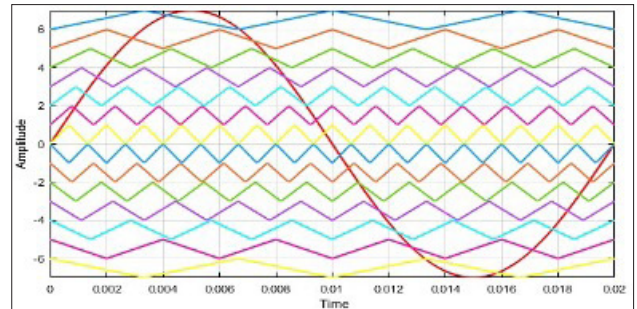


Figure 7. Triangular based multi-carrier VFCO-SPWM

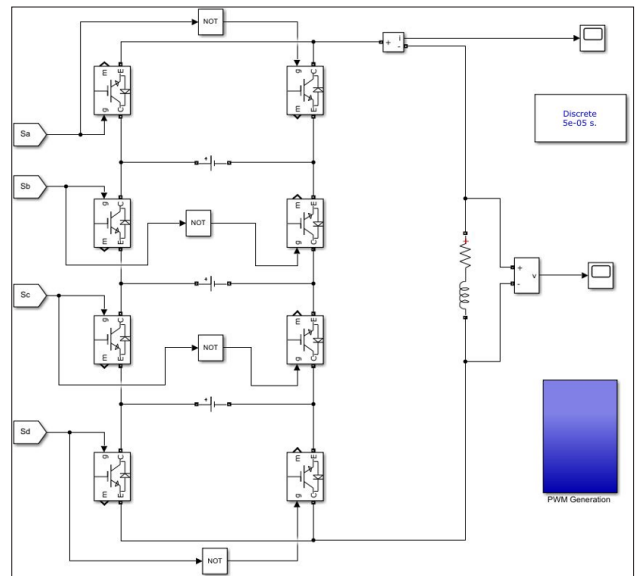


Figure 8. Simulation model of PUC-15 MLI

Table 4. Load parameters for PUC-15 MLI topology

Parameters	Specifications
DC source voltage (V _{dc})	V ₁ =230 V, V ₂ =99 V, V ₃ =33 V
Fundamental frequency	50 Hz
Switching frequency	3 kHz
Load resistance	40 Ω
Load inductance	3 mH
PUC-15: packed U cell 15 level; MLI: multilevel inverter	

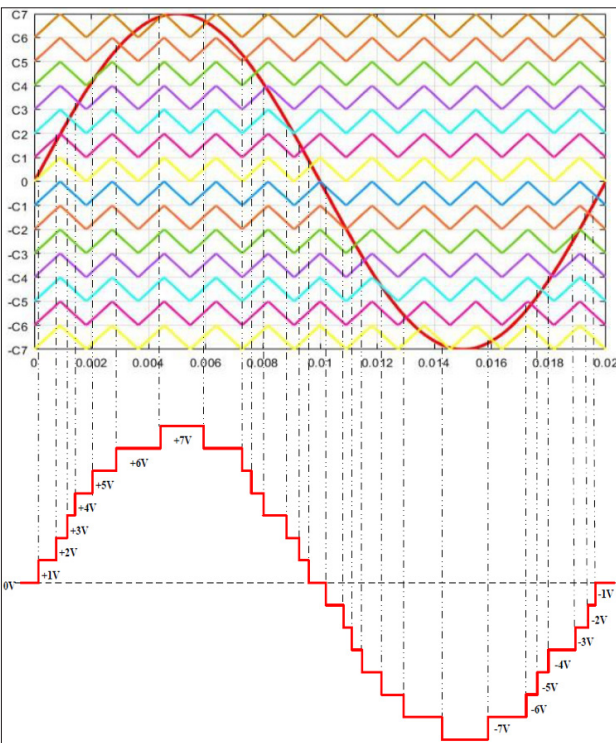


Figure 9. 15 level output generation with comparison of multi-carrier & sinewave for PUC MLI

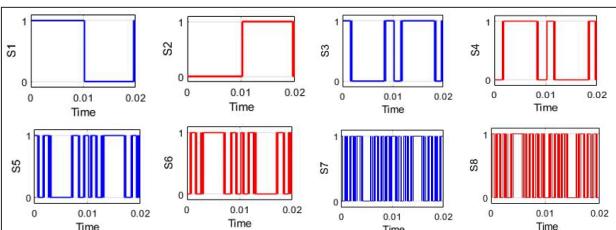


Figure 10. Switching pulses for PUC-15 MLI

15 level output voltages using modified switching sequences and PWM techniques. The switches S_1, S_3, S_5, S_7 (blue) pulse are normal and operate at different time periods; and the switches S_2, S_4, S_6, S_8 (red) pulses are complementary to switches S_1, S_3, S_5, S_7 of PUC-15.

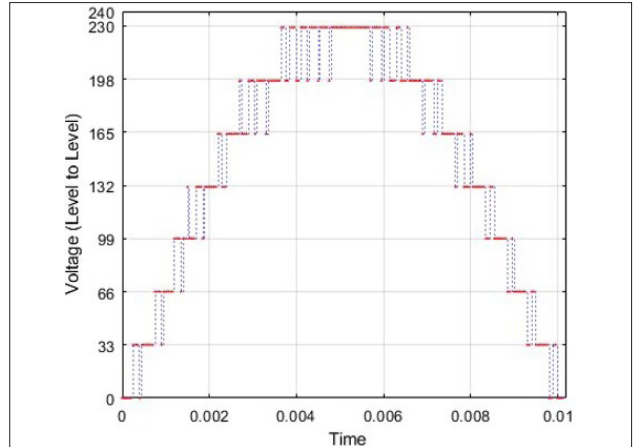


Figure 11. Half cycle output voltage waveform for PUC-15

Figure 11 exhibits only positive half-cycle output waveform of PUC-15. This waveform is helpful to find RMS voltage in a graphical analysis because MLIs are non-sinusoidal outputs.

Half-cycle for PUC-15 – seven voltage levels randomly rise, and seven voltage levels fall with same voltage increments and decrements at different time periods.

Peak voltage (V_p) = 230 (V), for 15-level voltages (7 steps up and 7 steps down)

$$V_{1p} = \frac{V}{7} = \frac{230}{7} = 32.85 \approx 33 \text{ (every step needs an increment of 33 volts)} \quad 15$$

Root mean square voltage for PUC can be calculated by using graphical analysis because MLIs are non-sinusoidal outputs.

$$V_{RMS} = \frac{\sqrt{\text{Sum \& square of voltage subordinates}}}{\sqrt{\text{Number of voltage subordinates}}} \quad 16$$

$$= \frac{\sqrt{(V_1^2 + V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + V_8^2 + V_9^2 + V_{10}^2 + V_{11}^2 + V_{12}^2 + V_{13}^2 + V_{14}^2 + V_{15}^2)}}{\sqrt{15}} \quad (15)$$

$$= \frac{\sqrt{(33^2 + 66^2 + 99^2 + 132^2 + 165^2 + 198^2 + 230^2 + 230^2 + 198^2 + 165^2 + 132^2 + 99^2 + 66^2 + 33^2 + 0^2)}}{\sqrt{15}} \quad (15)$$

$$V_{RMS} = 142.36 \quad 17$$

One half-cycle contain 15 time periods $T_p = 10 \text{ ms}$ ($T = 0.01$)

One pulse width time period $T_{1p} = \frac{T}{15} = 0.0006666$ (pulse to pulse 0.0006666 ms)

One half-cycle contain 15 different firing angles $\theta_a = 180^\circ$

One firing angle for one pulse width $\theta_{1a} = \frac{180^\circ}{15} = 12^\circ$ (every pulse to pulse varies at a 12° firing angle)

Table 5 represents firing angles for every peak voltage. All peak voltages are represented in the middle of the table. At V_p the voltage is 33V₁ with a voltage firing angle and decrement firing angle of 12° and 168° , respectively, before and after the time period of 0.005 ms.

Table 5. Firing angles for PUC-15 MLI topology at peak voltage

Voltage increment angle	Peak voltage (Vp)	Voltage decrement angle
0°	0	180°
12°	33	168°
24°	66	156°
36°	99	144°
48°	132	132°
60°	165	120°
72°	198	108°
84°	230	96°

PUC-15: packed U cell 15 level; MLI: multilevel inverter

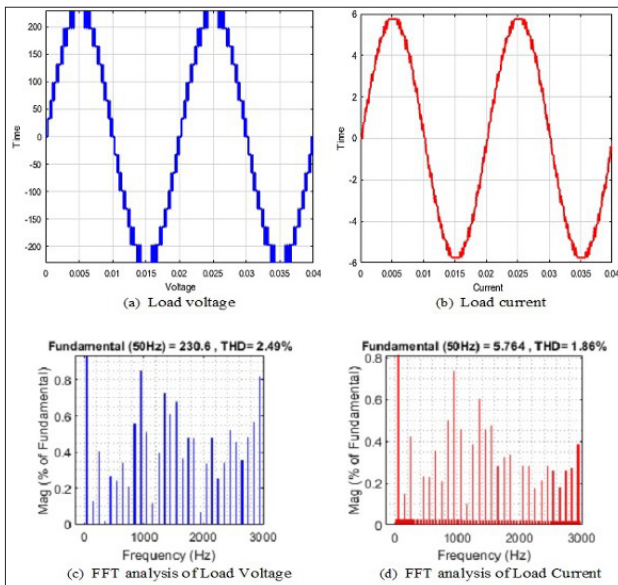


Figure 12. Performances analysis of PUC-15 MLI based on PD-SPWM

Phase Disposition Triangular Based Multi-Carrier SPWM Technique (PD-SPWM)

The simulation results in Figure 12 (a-d) represent the load voltage, load current output waveforms, and THD analysis presented at MI 1.0. The THD values of the phase voltage and currents are 2.49% and 1.86%, respectively.

Phase Opposition Disposition Triangular based Multi-Carrier SPWM technique (PS-SPWM)

The simulation results in Figure 13 (a-d) represent the load voltage, load current output waveforms, and THD analysis presented at MI 1.0. The THD values of the phase voltage and currents are 4.19% and 2.48%, respectively.

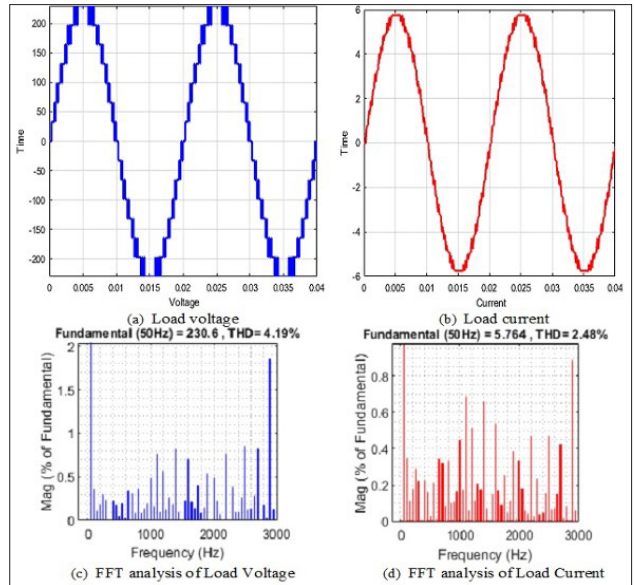


Figure 13. Performances analysis of PUC-15 MLI based on POD-SPWM

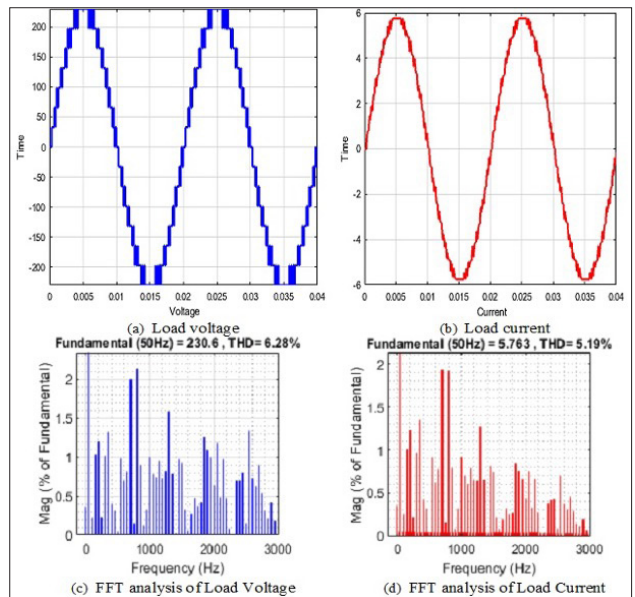


Figure 14. Performances analysis of PUC-15 MLI based on VF-SPWM

Variable Frequency Triangular Carrier-based PWM Technique (VF-SPWM)

The simulation results in Figure 14 (a-d) represent the load voltage, load current output waveforms, and THD analysis presented at MI 1.0. The THD values of the phase voltage and currents are 6.28% and 5.19%, respectively.

Variable Frequency Carrier Opposition Triangular Carrier-based PWM Technique (VFCO-SPWM)

The simulation results in Figure 15 (a-d) represent the load voltage, load current output waveforms, and THD analysis present-

ed at MI 1.0. The THD values of the phase voltage and currents are 5.88% and 4.68%, respectively.

Performance Analysis

The THD percentage of PUC-15 MLI was analyzed in terms of Fast Fourier Transform analysis using different PWM techniques at modulation index of M = 1, 0.8, 0.6, 0.4, and 0.2. Table 4 compares the THD percentage of PUC-15 for different PWM techniques at M = 1. Tables 6–11 represent the same at M = 0.8, 0.6, 0.4, and 0.2, respectively; and Figures (12–15) represent the THD graph analysis for PD-PWM, POD-PWM, VF-PWM, VF-CO-PWM at M = 0.8, 0.6, 0.4, and 0.2, respectively, for load voltage and load currents.

The modulation index is defined by $M = \frac{A_r}{A_c}$ where A_r = reference signals for amplitude and A_c = carrier signals for amplitude.

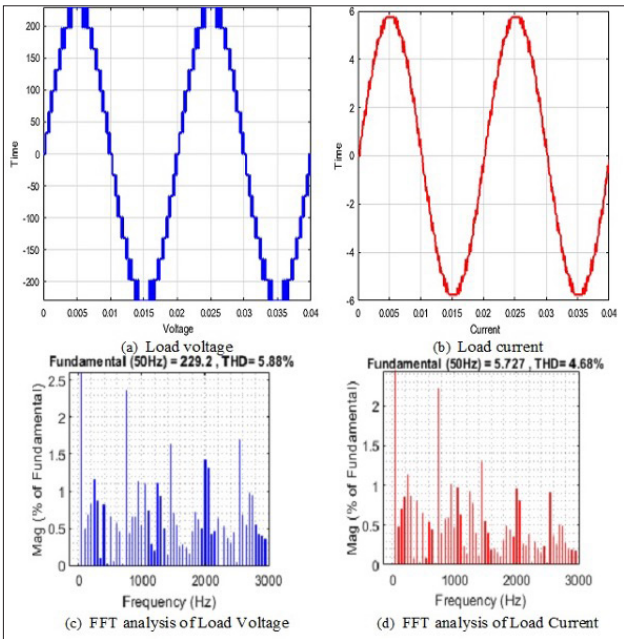


Figure 15. Performances analysis of PUC-15 MLI based on VF-CO-SPWM

Table 6. Comparison of THD percentages of PUC-15 for different PWM techniques at M = 1

THD	Triangular PWM			
	Constant frequency	Variable frequency		
	PD	POD	VF	VFCO
Load voltage	2.49	4.19	6.28	5.88
Load current	1.86	2.48	5.19	4.68

PUC-15: packed U cell 15 level; THD: total harmonic distortion; PWM: pulse width modulation; PD: phase disposition; POD: phase opposition disposition; VF: variable frequency; VFCO: variable frequency carrier opposition

The overall performances of PWM techniques were analyzed for constant and variable frequencies using Tables 6-11 and Figures 16 (a-f). It is evident that at a constant frequency, the PD-SPWM technique has a THD of 2.49% and 1.86% at M = 1; 3.26% and 2.38% at M = 0.8; 4.66% and 3.42% at M = 0.6; 6.41% and 4.21% at M = 0.4; 11.63% and 7.48% at M = 0.2, respectively, for load voltage and load currents. The POD-SPWM technique has a THD of 4.19% and 2.48% at M = 1; 6.80% and 3.65% at M = 0.8; 7.50% and 4.40% at M = 0.6; 13.04% and 6.71% at M = 0.4; 22.86% and 11.98% at M = 0.2, respectively, for load voltage and load currents. At VF, the VF-SPWM technique has a THD of 6.28% and 5.19% at M = 1; 8.20% and

Table 7. Comparison of THD percentage of PUC-15 for different PWM techniques at M = 0.8

THD	Triangular PWM			
	Constant frequency	Variable frequency		
	PD	POD	VF	VFCO
Load voltage	3.26	6.80	8.20	8.55
Load current	2.38	3.65	6.48	6.66

THD: total harmonic distortion; PWM: pulse width modulation; PD: phase disposition; POD: phase opposition disposition; VF: variable frequency; VFCO: variable frequency carrier opposition

Table 8. Comparison of THD percentage of PUC-15 for different PWM Techniques at M = 0.6

THD	Triangular PWM			
	Constant frequency	Variable frequency		
	PD	POD	VF	VFCO
Load voltage	4.66	7.50	7.87	7.80
Load current	3.42	4.40	5.18	5.09

THD: total harmonic distortion; PWM: pulse width modulation; PD: phase disposition; POD: phase opposition disposition; VF: variable frequency; VFCO: variable frequency carrier opposition

Table 9. Comparison of THD percentage of PUC-15 for different PWM Techniques at M = 0.4

THD	Triangular PWM			
	Constant frequency	Variable frequency		
	PD	POD	VF	VFCO
Load voltage	6.41	13.04	8.23	9.58
Load current	4.21	6.71	4.74	5.31

THD: total harmonic distortion; PWM: pulse width modulation; PD: phase disposition; POD: phase opposition disposition; VF: variable frequency; VFCO: variable frequency carrier opposition

6.48% at $M = 0.8$; 7.87% and 5.18% at $M = 0.6$; 8.23% and 4.74% at $M = 0.4$; 9.78% and 7.26% at $M = 0.2$, respectively, for load voltage and load currents. The VF-CO-SPWM technique has low THD values of 5.88% and 4.68% at $M = 1$; 8.55% and 6.66% at $M = 0.8$; 7.80% and 5.09% at $M = 0.6$; 9.58% and 5.31% at $M = 0.4$; 10.56% and 7.93% at $M = 0.2$, respectively, for load voltage and load current, as shown in Table 9. These are also evident axiomatically when the modulation index M is increased. The THD percentage is reduced randomly in constant frequency SPWM methods, and PD-SPWM technique has lower THD percentage at $M = 1$, thereby proving that the modified switching sequence also works perfectly for the respective PWM techniques.

Conclusion

In this study, the performance of PUC-15 MLI with modified switching sequence was analyzed using numerical analyses and simulations. The proposed switching sequence has benefits including an improved harmonic spectrum, optimized switching sequence obtained by controlling the burden on the switch, and controlled switching frequency compared with other conventional multilevel inverters. The simulated results are compared with advanced triangular carrier-based PWM

techniques with constant frequencies (PD, POD) and variable frequencies (VF, VF-CO) at different modulation indices of $M = 0.2, 0.4, 0.6, 0.8$, and 1. The advanced carrier-based PD modulation technique produces better results than the POD, VF, and VF-CO-PWM techniques in terms of %THD—the voltage and current THDs are 2.49% and 1.86% at $M = 1$, and these come under the IEEE-519 standard.

Table 10. Comparison of THD percentage of PUC-15 for different PWM Techniques at $M = 0.2$

THD	Triangular PWM			
	Constant frequency		Variable frequency	
	PD	POD	VF	VF-CO
Load voltage	11.63	22.86	9.78	10.56
Load current	7.48	11.98	7.26	7.93

THD: total harmonic distortion; PWM: pulse width modulation; PD: phase disposition; POD: phase opposition disposition; VF: variable frequency; VF-CO: variable frequency carrier opposition

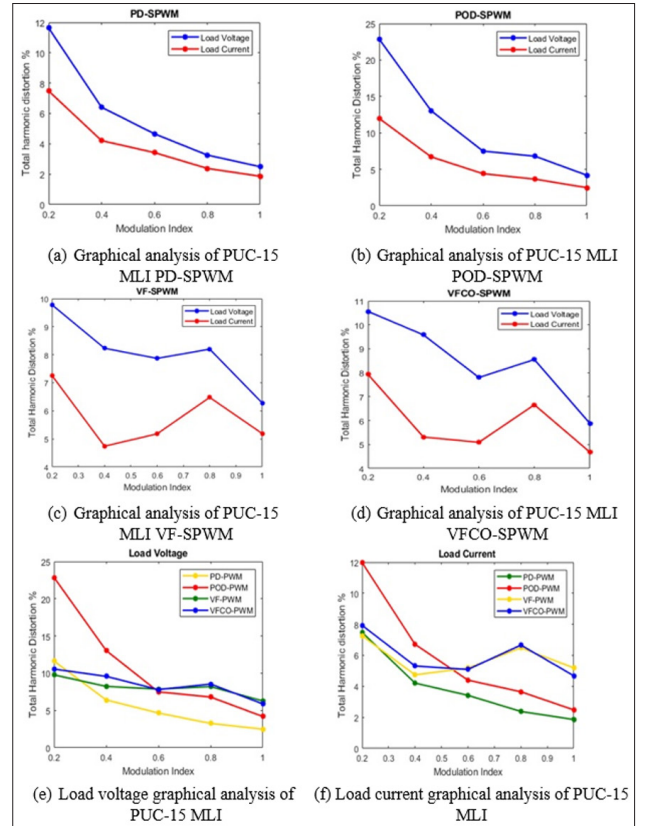


Figure 16. Graphical analysis of PUC-15 MLI using SPWM techniques

Table 11. Comparison of THD percentage of PUC-15 for different PWM Techniques at $M = (1.0 \text{ to } 0.2)$

MI	Triangular PWM							
	Constant frequency				Variable frequency			
	PD		POD		VF		VFCO	
	Load voltage	Load current	Load voltage	Load current	Load voltage	Load current	Load voltage	Load current
1.0	2.49	1.86	4.19	2.48	6.28	5.19	5.88	4.68
0.8	3.26	2.38	6.80	3.65	8.20	6.48	8.55	6.66
0.6	4.66	3.42	7.50	4.40	7.87	5.18	7.80	5.09
0.4	6.41	4.21	13.04	6.71	8.23	4.74	9.58	5.31
0.2	11.63	7.48	22.86	11.98	9.78	7.26	10.56	7.93

MI: modulation index; PWM: pulse width modulation; PD: phase disposition; POD: phase opposition disposition; VF: variable frequency; VF-CO: variable frequency carrier opposition

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