İSTANBUL UNIVERSITY CERRAHPAŞA

ORIGINAL ARTICLE
Electrica 2022; 22(1): 27-40

Minimized Total Harmonic Distortion of a Multi-level Inverter of a Wind Power Conversion Chain Synchronized to the Grid-LCL Filter Optimization and Third Harmonic Cancellation

Wijdane El Maataoui[1], Soukaina El Daoudi[2], Loubna Lazrak[2], Mustapha Mabrouki[1]

[1]Laboratory of Industrial Engineering, Faculty of Sciences and Technology, Sultan Moulay Slimane University, Beni-Mellal, Morocco
[2]Laboratory of Automatic, Energy Conversion and Microelectronics, Faculty of Sciences and Technology, Sultan Moulay Slimane University, Beni-Mellal, Morocco

Cite this article as: W. El Maataoui, S. El Daoudi, L. Lazrak, and M. Mabrouki, "Minimized total harmonic distortion of a multi-level inverter of a wind power conversion chain synchronized to the grid-LCL filter optimization and third harmonic cancellation," *Electrica*, 22(1), 27-40, Jan. 2022.

ABSTRACT

In order to improve the wind power conversion chain performance on the grid side, this work proposes the use of multi-level inverter and a fairly high switching frequency for an optimized LCL filter, while respecting the grid connection conditions. The method used consists of reducing the total harmonic distortion and adjusting filter parameters to cancel the third order harmonic. For grid-side chain control, two cascaded current and voltage control loops are used to generate the inverter pulse width modulation. To ensure synchronization even in the presence of grid faults or unbalance, a phase-locked loop (PLL) circuit with a multi-variable band-pass filter (MVBPF) is adopted. To validate the theoretical study, simulations are performed for a 300 W chain with a two-level, three-level, and five-level inverter using three different filters. A comparative study of the results shows that the use of the five-level inverter with the optimized filter effectively reduces ripples while meeting grid coupling conditions.

***Index Terms*—**LCL filter, multi-level inverters, multi-variable band-pass filter (MVBPF), phase-locked loop (PLL), sinusoidal pulse width modulation (SPWM), total harmonic distortion (THD), wind turbine conversion chain.

I. INTRODUCTION

According to the "World Energy Outlook 2015" study by the International Energy Agency (IEA), about 67% of the world's electricity is generated from fossil fuels which constitute the main source of electricity produced globally [1]. However, the negative environmental impacts of fuel-based electricity generation, climate change, depletion of fossil fuel reserves, and price fluctuations require the increased use of renewable energy for electricity supply worldwide [2, 3]. The use of wind energy for power generation was developed in the early 20th century, making it the most promising clean and sustainable energy source [4]. Globally, wind energy has been growing at a rate of 30% per year for the past decade [5]. According to the Global Wind Energy Council (GWEC), 2020 was the best year in history for the global wind industry, with 93 GW of newly installed capacity [6]. The principle of the wind turbine generator is to use the kinetic energy of wind to drive the rotor shaft and thus transform it into mechanical energy, which is converted into electrical energy by means of an electromagnetic generator [7]. Several types of electrical machines can be inserted in the wind turbine conversion chain, adjusted to the chosen installation control. The specifications for wind generators vary according to the type and geometric dimensions of the wind turbine, where the synchronous machine can be used in the case of direct drive [8]. The electrical energy produced by the wind turbine can be stored by accumulators, distributed through a power grid, or absorbed by isolated loads. Static converters such as inverters are an important part of the electrical energy conversion chain and have a strong influence on the quality of the produced energy. In recent years, the use of multi-level converters for power electronic applications has seen increasing demanded due to their many advantages, especially in the medium and high-power range [9-11]. The control of the inverter switches directly impacts the total harmonic distortion (THD) and the switching losses of the inverter [12]. Among the techniques used is the sinusoidal pulse width modulation (SPWM). This method has a simple structure to manipulate with a very low computation time, while pushing

Corresponding Author:
Wijdane El Maataoui

E-mail:
elmaataoui.wijdane@gmail.com

Received: July 14, 2021

Revised: October 2, 2021

Accepted: October 8, 2021

Available Online Date: November 17, 2021

DOI: 10.5152/electrica.2021.21086

the harmonics to high frequencies, which makes filtering much easier [13]. The insertion of a filter satisfies the conditions of coupling with the grid, and the most commonly employed filters are L, LC, and LCL. The major disadvantage of the L filter is the large value of the inductance which leads to high voltage drops [14]. However, the use of an LC filter is not recommended for renewable energy conversion systems due to the direct connection instability of the capacitor in parallel with the grid [15]. The LCL structure presents an alternative that reduces its parameter dimensions and increases attenuation. However, the disadvantage of this filter design is the resonance, which can be reduced by inserting a resistor in parallel or in series with the capacitor and inductors [16]. Nonetheless, a connection with the grid requires good synchronization, where the amplitude, frequency, and phase angle of the grid voltage are the three essential elements to ensure it. The phase-locked loop (PLL) is widely used to achieve the aforementioned components [17]. Several synchronization circuit structures are used in the literature such as zero-crossing detection (dq-PLL), direct system extraction of voltages with dq-PLL (PSD-dq-PLL), and filtering of measured voltages with dq-PLL (FMVPB-dq-PLL) [18]; the interest of this last structure is to ensure a good synchronization with the grid even in the presence of faults or unbalance of the latter [19, 20].

In order to improve the wind conversion chain, [21] proposed a comparative study of various methods to optimize the LCL filter. However those techniques have many disadvantages such as complex design and non-fulfillment of the imposed performance indexes. Furthermore, very few research studies have been done in analyzing performance of the conversion chain while using a multi-level inverter and an optimized LCL filter at the same time.

Thus, the main contributions of the present work are about designing an optimized LCL filter, PLL synchronization on the grid side with multi-variable band pass filter (FMVPB-dq-PLL), and the use of a multi-level inverter, especially the three-level and five-level inverters. A consistent comparative study has been made with three inverter topologies and three designs of the LCL filter.

The method of optimizing the LCL filter parameters is suggested to improve the output magnitudes by cancelling the third order harmonic. The use of the five-level inverter with the optimized LCL filter and FMVPB-dq-PLL allows a great THD mitigation, and a remarkable reduction of the installation cost while meeting the requirements of grid connection.

The paper is structured as follows: the architecture of the power conversion chain with the two-level inverter, the sizing of the LCL filter, the closed-loop control, as well as the FMVPB-dq-PLL synchronization are represented in Section 2. Sections 3 and 4 are devoted to the conversion chain with the three-level and five-level inverters respectively, and their balancing loops are also presented. Sections 5 and 6 discuss the methods adopted to optimize the filter and to cancel the third order harmonic. The simulation results are presented and discussed in Section 7, before closing with a general conclusion in Section 8.

II. STRUCTURE OF THE ENERGY CONVERSION CHAIN WITH THE USUAL TWO-LEVEL INVERTER

Fig. 1 shows the schematic diagram of the power conversion chain on the grid side. It consists of a two-level inverter, an LCL filter, an internal current regulation loop, an external voltage regulation loop, and an FMVPB-dq-PLL synchronization loop.

A. Two-level Inverter

Fig. 1 shows the topology of the two-level inverter, which is composed of three arms with two electronic switches, with antiparallel protection diodes placed in each of them to ensure freewheeling. The switch type used depends on the inverter power and the switching frequency. In most applications, IGBT transistors with antiparallel diodes are employed since they have high efficiency and good robustness. The inverter is powered by a DC voltage source, either from three-phase diode rectifier or from batteries [10].

The triangle sine pulse width modulation (SPWM) is realized by comparing a low-frequency modulating wave (reference voltage) to a high-frequency triangular carrier wave. The switching times are determined by the intersection points between the carrier and the modulating waves.

B. LCL Filter Design

The LCL filter remains the right choice compared to the other filters mentioned in the literature, since it represents an attenuation of 60 dB/decade and its resonance is independent of the grid impedance.

This filter can be modeled by three identical single-phase electrical diagrams, presented in Fig. 2.

To solve the resonance problem produced by LCL filter at its cutoff frequency, it is necessary to insert a real damping resistor in the passive case and a virtual damping resistor in the active case.

The single-phase modeling of the LCL filter can be represented as follows:

$$\begin{cases} i_1 = i_2 + i_c \\ v_i = \left(R_i + sL_i\right) i_1 + v_c \\ v_c = \left(R_g + sL_g\right) i_2 + v_g \\ v_c = i_c \left(\frac{1}{sC} + R_c\right) \end{cases}. \quad (1)$$

In the low-frequency range, the LCL filter behaves like an L-filter, thus the LCL filter can be remodeled by neglecting the filtering capacity C:

$$\begin{cases} i_1 = i_2 = i \\ v_i = \left(R_i + sL_i\right) i_1 + v_c \\ v_c = \left(R_g + sL_g\right) i_2 + v_g \end{cases}. \quad (2)$$

Considering the output voltage as an ideal source ($v_g = 0$), the expression of the transfer function of the filter is presented as follows:

$$\frac{i(s)}{v_i(s)} = \frac{1}{\left(R_i + R_g\right) + s\left(L_i + L_g\right)}. \quad (3)$$

The impedance and base capacitance are defined as [22]:

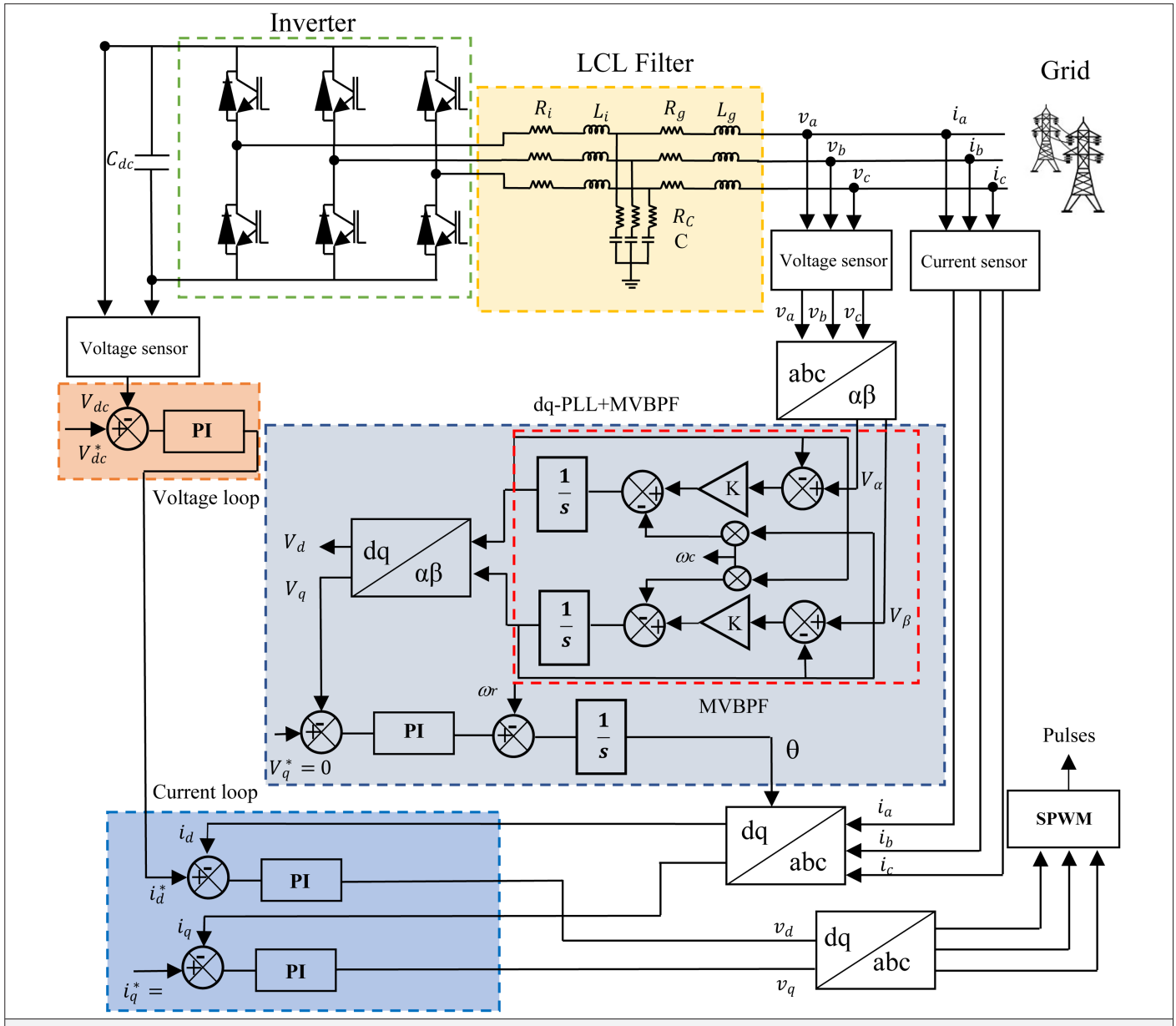


Fig. 1. Schematic diagram of the power conversion chain on the grid side with the two-level inverter.

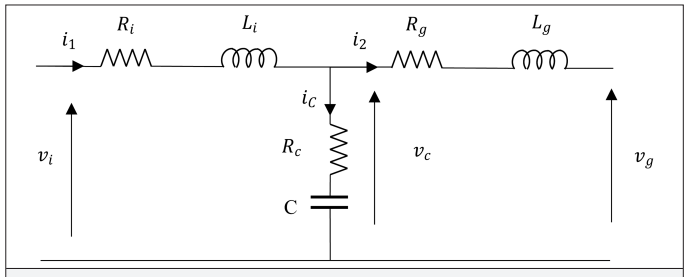


Fig. 2. Representation of the single-phase electrical circuit of the LCL filter with the passive damping resistor.

$$\begin{cases} Z_b = \dfrac{E_n^{\,2}}{S_n} \\ C_b = \dfrac{1}{\omega Z_b} \end{cases} \tag{4}$$

where S_n is the nominal apparent power and E_n is the nominal voltage.

Assuming that the maximum variation of the power factor from the grid side is equal to 10%, we get the following expression:

$$C = 0.1 * \frac{S_n}{\omega E_n^2}. \tag{5}$$

TABLE I. LCL1 FILTER PARAMETERS WITH 5 KHZ AND 10 KHZ SWITCHING FREQUENCIES

	R_i (Ω)	L_i (H)		R_c (Ω)	C (μF)	R_g (Ω)	L_g (H)	
		5 kHz	10 kHz				5 kHz	10 kHz
LCL1	200	2.07	1.04	160.51	0.66	8	$9.21*10^{-3}$	$2.30*10^{-3}$

The maximum current ripple at the output of the inverter is given by [22]:

$$\Delta I_{\max} = \frac{2V_{dc}}{3L_i}(1-m)mT_{sw} \tag{6}$$

where m is the modulation factor of the inverter and T_{sw} is the switching period.

For m = 0.5, the maximum peak-to-peak ripple of the current is:

$$\Delta I_{\max} = \frac{V_{dc}}{6f_{sw}L_i} \tag{7}$$

where L_i is the inductance on the inverter side, f_{sw} is the switching frequency, and v_{dc} is the DC voltage.

A ripple of 1% of the nominal current is chosen to the design the filter parameters:

$$\Delta I_{\max} = 0.01*I_{\max} \tag{8}$$

with $I_{\max} = \frac{P_n\sqrt{2}}{3E_{ph}}$

where P_n is the active power and E_{ph} is the phase voltage.

Therefore, the expression of the inductance on the inverter side is:

$$L_i = \frac{V_{dc}}{6f_{sw}\Delta I_{\max}}. \tag{9}$$

The formula of the inductance on the grid side is written in the following form [22]:

$$L_g = \frac{\sqrt{\frac{1}{k_a^2}}+1}{C\omega_{sw}^2} \tag{10}$$

where k_a is the attenuation factor and ω_{sw} is the switching pulsation.

To calculate the inductance L_g, an attenuation factor of $k_a = 20\%$ is imposed.

The R_c resistor in series with the capacitor attenuates a part of the fluctuations at the switching frequency to avoid the resonance peak [22]:

$$R_c = \frac{1}{3\omega_{res}C} \tag{11}$$

with $\omega_{res} = \sqrt{\frac{L_i+L_g}{L_iL_gC}}$ and $10f_g < f_{res} < 0.5f_{sw}$

where f_g is the grid frequency and f_{sw} is the switching frequency.

Table I shows the filter parameters calculated for the frequencies 5 kHz and 10 kHz; according to the results, it is preferable to work with the 10 kHz switching frequency to gain on filtering.

C. Control Strategy

The control method used in this paper consists of two cascaded control loops; the first one concerns the voltage control loop and the second one presents the current control from the first loop.

1) Internal current regulation loop

The current control loops along the *d*-axis and *q*-axis have the same dynamics; therefore, the setting of the controller parameters is done only for the *d*-axis. Fig. 3 shows the internal current control loop.

The loop consists of PI regulator, control block, sampling block, transfer functions of the inverter, and the filter. The expressions that define each block are expressed afterward.

The transfer function of the PI corrector is:

$$H_{PI}(s) = \left(\frac{K_I + sK_P}{s}\right). \tag{12}$$

The control of the system is characterized by a transfer function of the first order, which is written in the following form:

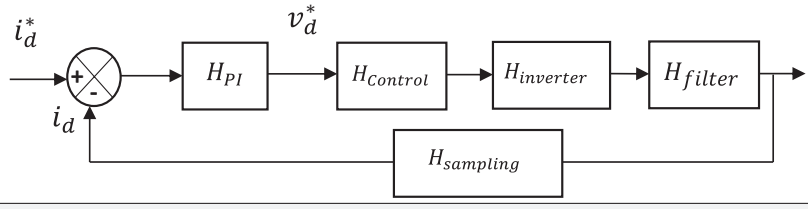


Fig. 3. Current control loop.

$$H_{Control}(s)=\frac{1}{1+sT_s} \tag{13}$$

where $T_s=\frac{1}{f_s}$ is the sampling time.

The transfer function of the inverter is formulated as follows:

$$H_{inverter}(s)=\frac{1}{1+sT_{sw}} \tag{14}$$

where T_{sw} is the switching period.

The LCL filter can be expressed by the following transfer function:

$$H_{filter}(s)=\frac{1}{sL_T+R_T}=\frac{K_e}{1+sT_e} \tag{15}$$

where $L_T=L_i+L_g$, $R_T=R_i+R_g$, $K_e=\frac{1}{R_T}$, and $T_e=\frac{L_T}{R_T}$.

The system has a sampling delay which is expressed in the following form:

$$H_{sampling}=\frac{1}{1+s*0.5T_s}. \tag{16}$$

Considering the control, inverter, and sampling transfer functions as delays, the open-loop transfer function of the internal current control loop is as follows:

$$H_{c,OL}=\frac{K_e\left(K_I+sK_P\right)}{s\left(1+sT_e\right)}. \tag{17}$$

The expression for the closed-loop transfer function of the current control can be written as follows:

$$H_{c,CL}=\frac{K_e/T_e\left(K_I+sK_P\right)}{s^2+\frac{1+K_eK_P}{T_e}s+\frac{K_eK_I}{T_e}}. \tag{18}$$

In order to determine the parameters K_p and K_i of the associated PI controller, the closed-loop transfer function is rewritten as a second order equation:

$$H(s)=\frac{2\xi\omega_n s+\omega_n^2}{s^2+2\xi\omega_n s+\omega_n^2} \tag{19}$$

where ω_n is the natural pulsation and ξ is the damping factor. For $\xi=\frac{\sqrt{2}}{2}$, an equivalent value of $\omega_n=\frac{3}{t_r}$ is associated with t_r which is the response time. By identification, K_p and K_i can be expressed as follows:

$$\begin{cases} K_I=L_T\omega_n^2 \\ K_P=2\xi\omega_nL_T-R_T \end{cases}. \tag{20}$$

2) External loop of the voltage regulation

The DC voltage loop, shown in Fig. 4, provides the reference current along the *d*-axis. It consists of PI control block, the closed-loop transfer function of the internal current loop, and the differential equation describing the voltage dynamics.

The DC intermediate circuit of the inverter is modeled as follows:

$$i_{dc}=C_{dc}\frac{dv_{dc}}{dt}+i_{inv}. \tag{21}$$

The active and reactive power exchanged between the inverter and the grid in the synchronous reference frame (*d*–*q*) are:

$$\begin{cases} P=\frac{3}{2}\left(v_di_d+v_qi_q\right)=v_{dc}i_{dc} \\ Q=\frac{3}{2}\left(v_qi_d-v_di_q\right) \end{cases}. \tag{22}$$

Assuming that the *d*-axis of the rotating marker is aligned with the AC voltage of the grid ($v_q=0$), the active and reactive power will be expressed as follows:

$$\begin{cases} P=\frac{3}{2}v_di_d \\ Q=-\frac{3}{2}v_di_q \end{cases}. \tag{23}$$

According to (21), (22), and (23), the dynamics of the DC voltage will be articulated as:

$$C_{dc}\frac{dv_{dc}}{dt}=\frac{3}{2}\frac{v_d}{v_{dc}}i_d-i_{inv}. \tag{24}$$

The closed-loop transfer function of the current can be written in the following form:

$$H_{c,CL}=\frac{1}{2sT_\Sigma\left(1+sT_\Sigma\right)+1}\approx\frac{0.5T_\Sigma+1}{2sT_\Sigma+1}$$

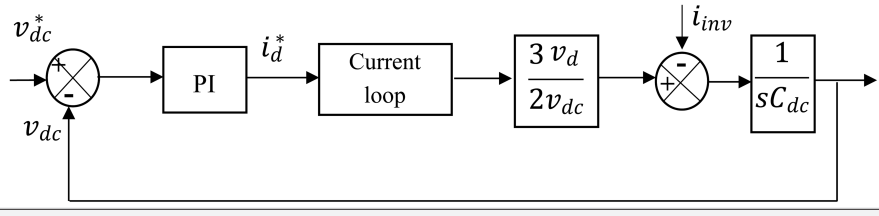


Fig. 4. Voltage control loop.

$$H_{c,CL} = \frac{0.5T_{\Sigma} + 1}{sT_{eq} + 1} \tag{25}$$

with $T_{eq} = 2T_{\Sigma}$ and $T_{\Sigma} = 2T_s$,

where Ts is the sampling period.

Therefore, the open-loop transfer function of the DC voltage in a simplified way is as follows:

$$H_{dc,OL} = K_{p\_dc}\left(\frac{1 + sT_{i\_dc}}{sT_{i\_dc}}\right)\frac{1}{sT_{eq} + 1}\frac{3}{2}\frac{v_d}{sC_{dc}v_{dc}}. \tag{26}$$

Applying the criterion of optimal symmetry, the parameters of the PI controller could be written as :

$$K_{p\_dc} = \frac{2v_{dc}C_{dc}}{3aT_{eq}v_d};\ T_{i\_dc} = a^2T_{eq} \text{ and a=3.}$$

Moreover, in steady state $v_d = v_{dc}$:

$$\text{Then}\begin{cases} K_{p\_dc} = \dfrac{2C_{dc}}{3aT_{eq}} = \dfrac{C_{dc}}{6aT_s} \\ K_{I\_dc} = \dfrac{C_{dc}}{72a^2{T_s}^2} \end{cases}. \tag{27}$$

C. dq-Phase-Locked Loop and Multi-variable Band-Pass Filter Synchronization

This PLL strategy is designed with a Multi-Variable Band-Pass Filter block (MVBPF) and the usual dq-PLL. By applying this structure, reliable frequency and phase detection will be achieved even if voltage imbalances and distortions are produced. The schematic diagram of the dq-PLL + MVBPF is shown in Fig. 5.

The filter, called the multi-variable filter can extract directly the fundamental signals (voltage or current) in the αβ axis without leading to either phase shift or change in voltage amplitude. However, it can also be used to reduce the direct and inverse harmonic components of input signals.

The equivalent transfer function of the integration in the synchronous reference frame is expressed by [20]:

$$v_{xy}(t) = e^{j\omega t}\int e^{j\omega t}u_{xy}(t)dt. \tag{28}$$

After Laplace transformation, the transfer function can be expressed as follows:

$$H(s) = \frac{V_{\alpha\beta f}(s)}{V_{\alpha\beta}(s)} = K_f\frac{(s + K_f) + j\omega_c}{(s + K_f)^2 + {\omega_c}^2} \tag{29}$$

$$\begin{cases} V_{\alpha f}(s) = \dfrac{K_f}{s}\left[V_{\alpha}(s) - V_{\alpha f}(s)\right] - \dfrac{\omega_c}{s}V_{\beta f}(s) \\ V_{\beta f}(s) = \dfrac{K_f}{s}\left[V_{\beta}(s) - V_{\beta f}(s)\right] - \dfrac{\omega_c}{s}V_{\alpha f}(s) \end{cases} \tag{30}$$

with:

ω_c : *Cut − off pulse*
K_f : *Dynamic gain*
$V_{\alpha\beta}$: *Input voltage*
$V_{\alpha\beta f}$: *Output voltage*

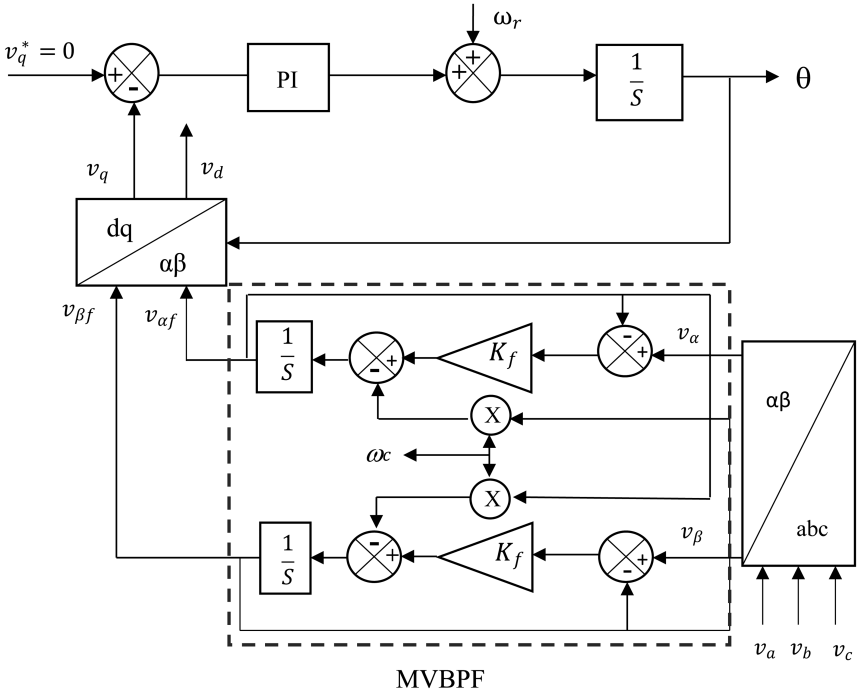


Fig. 5. dq-PLL + MVBPF synchronization.

III. CHAIN STRUCTURE WITH THE THREE-LEVEL NPC INVERTER

The power conversion chain with the three-level inverter, shown in Fig. 6, consists of a three-level inverter, an LCL filter, an internal current regulation loop, an external voltage regulation loop, and a dq-PLL synchronization loop, plus an MVBPF with a balancing loop.

A. NPC Three-Level Inverter

The main circuit of the three-phase three-level NPC inverter is shown in Fig. 6. This topology consists of three arms each with four power switches with two antiparallel diodes. Each phase shares a common DC bus, subdivided by two capacitors providing the neutral point N. The NPC reduces both current and voltage harmonics at the outputs [23]. The input DC bus of the three-level inverter is composed of two capacitors in series (C_1 and C_2), forming a midpoint that allows the inverter to access an additional voltage level compared to the conventional two-level inverter.

Sine pulse width modulation (SPWM), which is used to determine in real time the closing and opening states of the switches, consists of using the intersections of a reference wave, generally sinusoidal, with a triangular signal (known as the carrier). Two parameters characterize this control: the modulation rate and the modulation index [10].

B. Balancing Loop

The NPC inverter has an inherent problem of asymmetrical voltages across the DC link capacitors, a disadvantage which occurs due to the irregular charge/discharge and non-identical properties of the DC bus capacitors supplied by the manufacturer. For the three-level inverter, and in order to solve the above-mentioned anomaly, a balancing loop is required by putting $\frac{V_{dc}}{2} = V_{c1} = V_{c2}$.

The modulation signals are appropriately selected to generate the balanced AC voltage at the output terminals of the inverter.

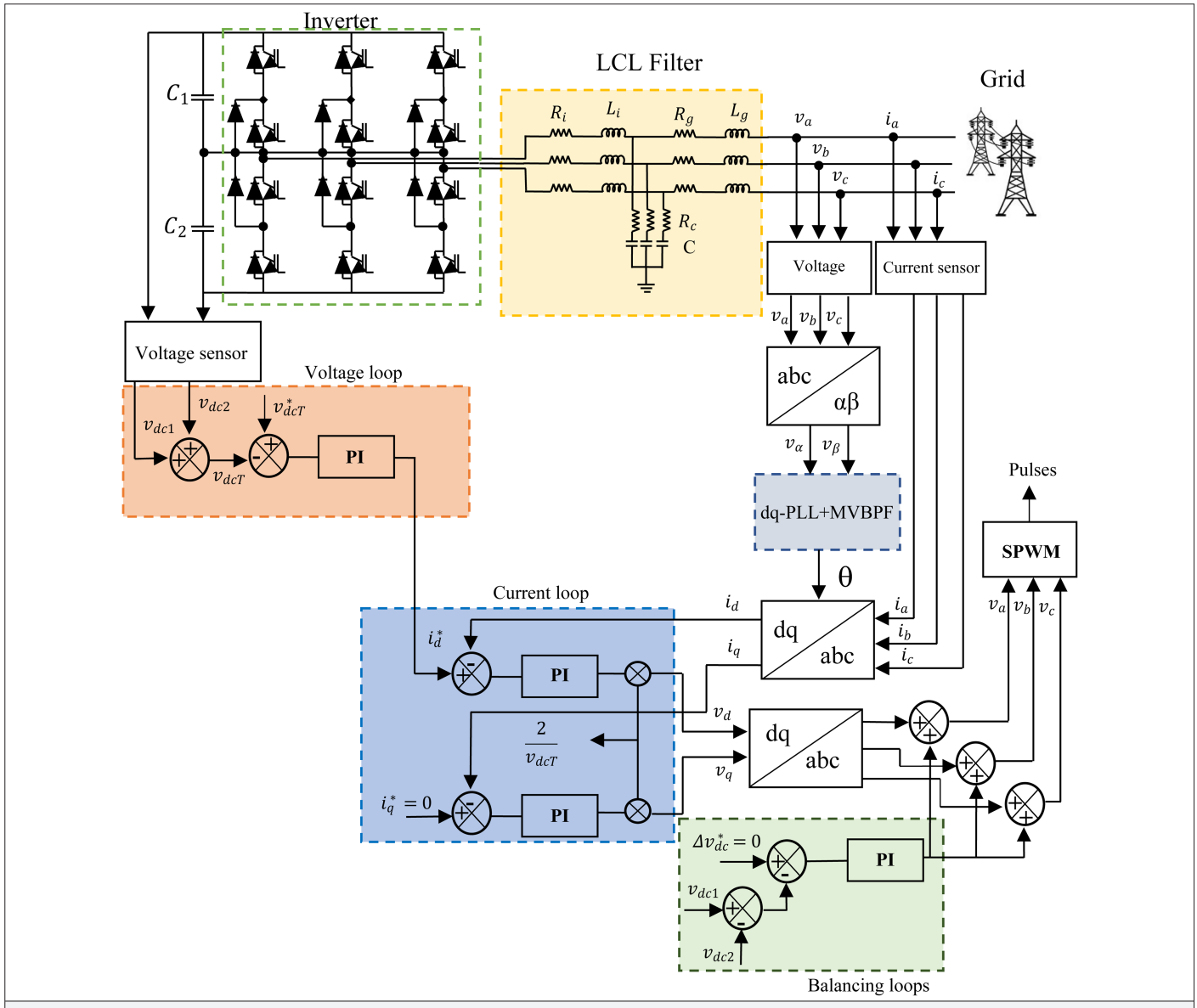


Fig. 6. Schematic diagram of the power conversion chain on the grid side with the three-level NPC inverter.

This balancing of the DC voltage of the inverter reduces the harmonic content and maintains the voltage stability in the neutral point [24].

IV. CHAIN STRUCTURE WITH THE FIVE-LEVEL INVERTER

The difference between the power conversion chain with the three-level NPC inverter and that with the five-level inverter is the balancing loop. The three-level NPC inverter adopts a single balancing loop, while the five-level inverter has three balancing loops.

A. Five-level Inverter

Multi-level inverters have been the subject of several researches in recent years and are now widely used in large and medium power conversion chains. These inverters are capable of minimizing total harmonic distortion and surge stress in the system by spreading the switching over multiple semiconductors [11]. Among the many multi-level topologies, the five-level blocking diode inverter is the most frequently used, consisting of three symmetrical arms each consisting of eight bidirectional switches in series with antiparallel diodes. These switches must not be opened or closed simultaneously, in order to avoid short-circuiting the DC source at the inverter's input. The number of blocking diodes is six per arm, ensuring the application of different voltage levels at the output. Each arm is connected to the DC supply V_{dc} which is divided into four equal parts using four capacitors (Fig. 7). This inverter is called five-level because it delivers five levels of the single output voltage $\left(\frac{V_{dc}}{2},\frac{V_{dc}}{4},0,-\frac{V_{dc}}{4},-\frac{V_{dc}}{2}\right)$.

The POD-PWM phase opposition technique uses four carrier signals to generate switching pulses. The carrier waves are in phase with a level above zero reference and the other two are taken with a phase shift of 180° below zero [11].

B. Balancing Loops

To solve the DC voltage unbalance problem across the four capacitors at the input of the five-level inverter, the control strategy requires three balancing loops to generate the control voltages of the SPWM with the condition $\frac{V_{dc}}{4}=V_{c1}=V_{c2}=V_{c3}=V_{c4}$.

V. FILTER OPTIMIZATION

From the simulation results of the first filter with the multi-level inverter, it can be concluded that the THD is decreased, thus a filter sizing minimization is possible by reducing inductances on the inverter and grid sides.

- *Inductance on the inverter side*

Following the relationships found in the LCL filter design section, the inductance on the inverter side can be optimized by increasing the ripple factor of the rated current $\left(\Delta I_{max}=0.013*I_{max}\right)$.

- *Inductance on the grid side*

The attenuation factor is a value to be imposed to perform the numerical calculation. In the case of the filter parameter optimization, $K_a=27\%$ is chosen.

VI. CONSTRAINT ON THE THIRD ORDER HARMONIC

According to Fig. 8 and 9 from simulation results section, the third order harmonic is preponderant. In order to eliminate this constraint, it is necessary to resize the filter by considering the star–delta conversion method. This latter consists of defining the filter parameters by cancelling the equivalent impedance for a pulse equal to three times the fundamental pulse. Fig. 10 shows the principal star configuration of the LCL filter.

In order to determine the elements of the LCL filter presented earlier, an equivalent triangle configuration is proposed (Fig. 11).

The impedances of the LCL filter in star configuration are presented as follows:

$$\begin{cases}\overline{z_a}=R_i+jL_i\omega\\ \overline{z_b}=R_g+jL_g\omega.\\ \overline{z_c}=R_C+\dfrac{1}{jC\omega}\end{cases}\tag{31}$$

By making the star–delta conversion equality of the two previous circuits, the expressions of the impedances of the delta circuit are then written as:

$$\overline{Z_A}=\frac{\overline{N}}{\overline{z_a}};\overline{Z_B}=\frac{\overline{N}}{\overline{z_b}};\overline{Z_C}=\frac{\overline{N}}{\overline{z_c}}\tag{32}$$

with

$$\overline{N}=\overline{z_a}\overline{z_b}+\overline{z_b}\overline{z_c}+\overline{z_c}\overline{z_a}.\tag{33}$$

By replacing the impedances $\overline{z_a}$, $\overline{z_b}$, and $\overline{z_c}$ by their expressions, the new formula of $\overline{N}$ is:

$$\begin{aligned}\overline{N}&=\overline{z_a}\overline{z_b}+\overline{z_b}\overline{z_c}+\overline{z_c}\overline{z_a}\\&=\left(R_i+jL_i\omega\right)\left(R_g+jL_g\omega\right)+\left(R_g+jL_g\omega\right)\left(R_C+\frac{1}{jC\omega}\right)\\&+\left(R_C+\frac{1}{jC\omega}\right)\left(R_i+jL_i\omega\right)\\&=\left[R_iR_g+jR_iL_g\omega+jR_gL_i\omega-L_iL_g\omega^2\right]\\&+\left[R_gR_C+\frac{R_g}{jC\omega}+jL_g\omega R_C+\frac{L_g}{C}\right]\\&+\left[R_CR_i+jR_CL_i\omega+\frac{R_i}{jC\omega}+\frac{L_i}{C}\right]\\&=\left[\left(R_iR_g-L_iL_g\omega^2\right)+\left(R_gR_C+\frac{L_g}{C}\right)+\left(R_CR_i+\frac{L_i}{C}\right)\right]\\&+j\left[\left(R_iL_g\omega+R_gL_i\omega\right)+\left(L_gR_C\omega-\frac{R_g}{C\omega}\right)+\left(R_CL_i\omega-\frac{R_i}{C\omega}\right)\right].\end{aligned}\tag{34}$$

The expression for the equivalent impedance of the delta circuit is:

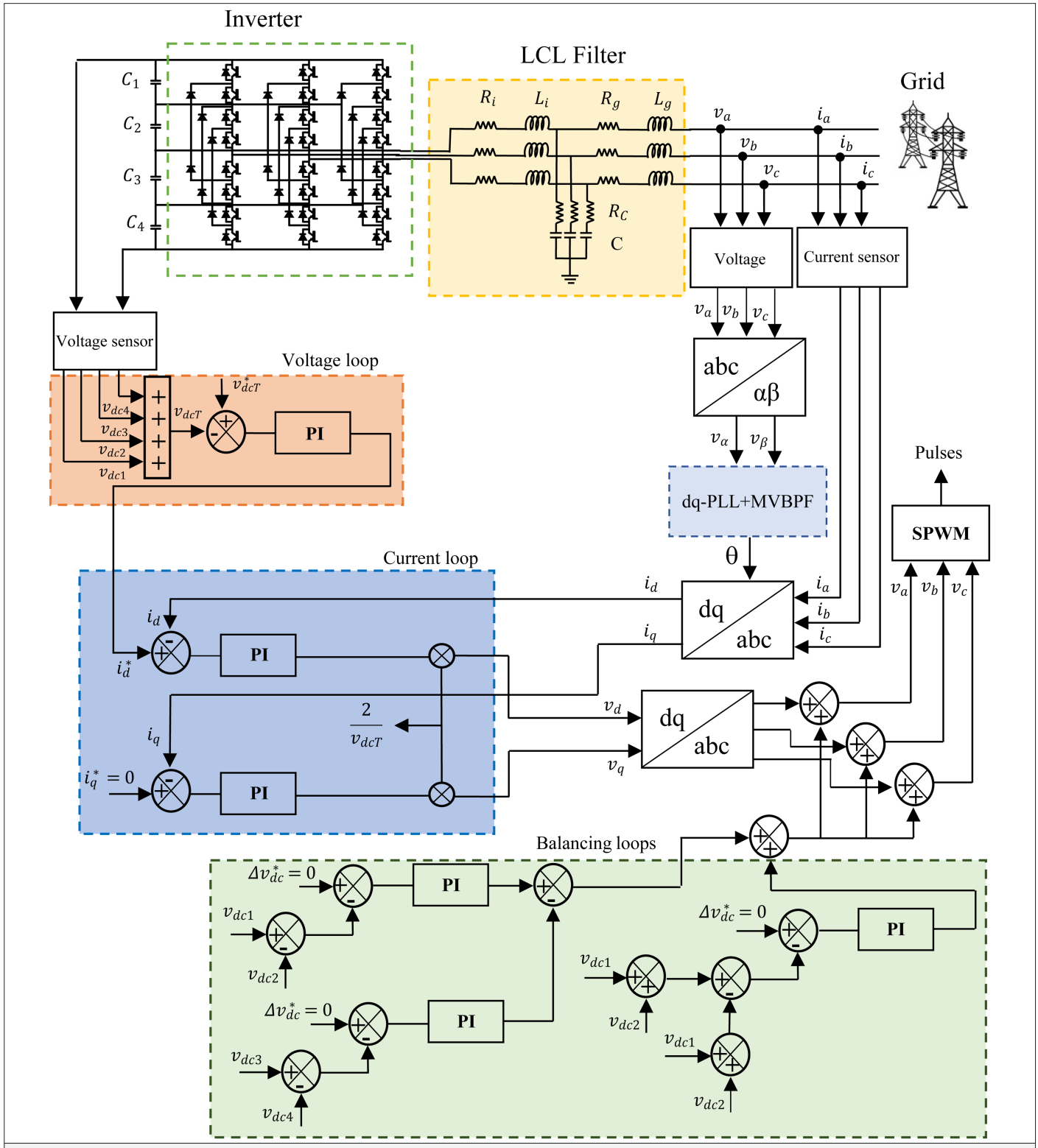


Fig. 7. Schematic diagram of the grid-side power conversion chain with the five-level inverter.

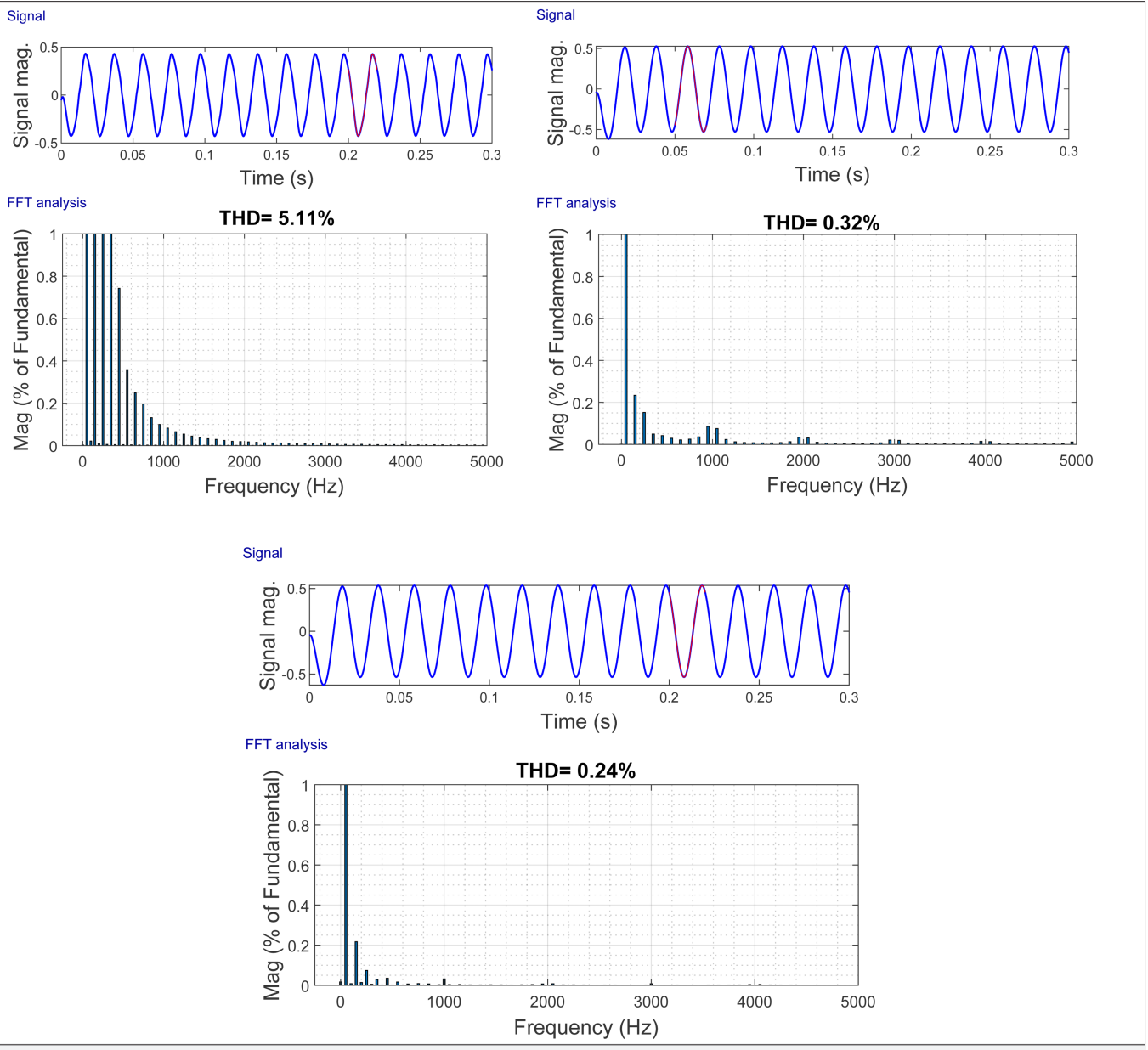


Fig. 8. Spectral analysis of the output current of the first filter with the (a) two-level, (b) three-level, and (c) five-level inverters.

$$\overline{Z_{eq}} = \overline{Z_B} \| \left(\overline{Z_C} + \overline{Z_A} \right) = \frac{\overline{Z_B} \left(\overline{Z_C} + \overline{Z_A} \right)}{\overline{Z_A} + \overline{Z_B} + \overline{Z_C}} = \frac{\overline{N^2} \left(\overline{z_a} + \overline{z_c} \right)}{\overline{z_b z_c} N + \overline{z_a z_c} N + \overline{z_a z_b} N}. \quad (35)$$

To cancel the third order harmonic, the LCL filter parameters are calculated in order to have $\overline{Z_{eq}} = 0$ for $\omega_h = 3\omega$:

$$\overline{Z_{eq}} = 0 \Rightarrow \overline{N^2} \left(\overline{z_a} + \overline{z_c} \right) = 0. \quad (36)$$

The grid-side inductance is expressed as:

$$L_g = \frac{\frac{R_g}{C\omega} + \frac{R_i}{C\omega} - R_g L_i \omega - R_C L_i \omega}{\left(R_i \omega + R_C \omega \right)}. \quad (37)$$

The inductance and resistance on the inverter side will be defined as follows:

$$\begin{cases} R_i = R_C \\ L_i \omega - \frac{1}{C\omega} = 0 \Rightarrow L_i = \frac{1}{C \left(3\omega_n \right)^2} \end{cases}. \quad (38)$$

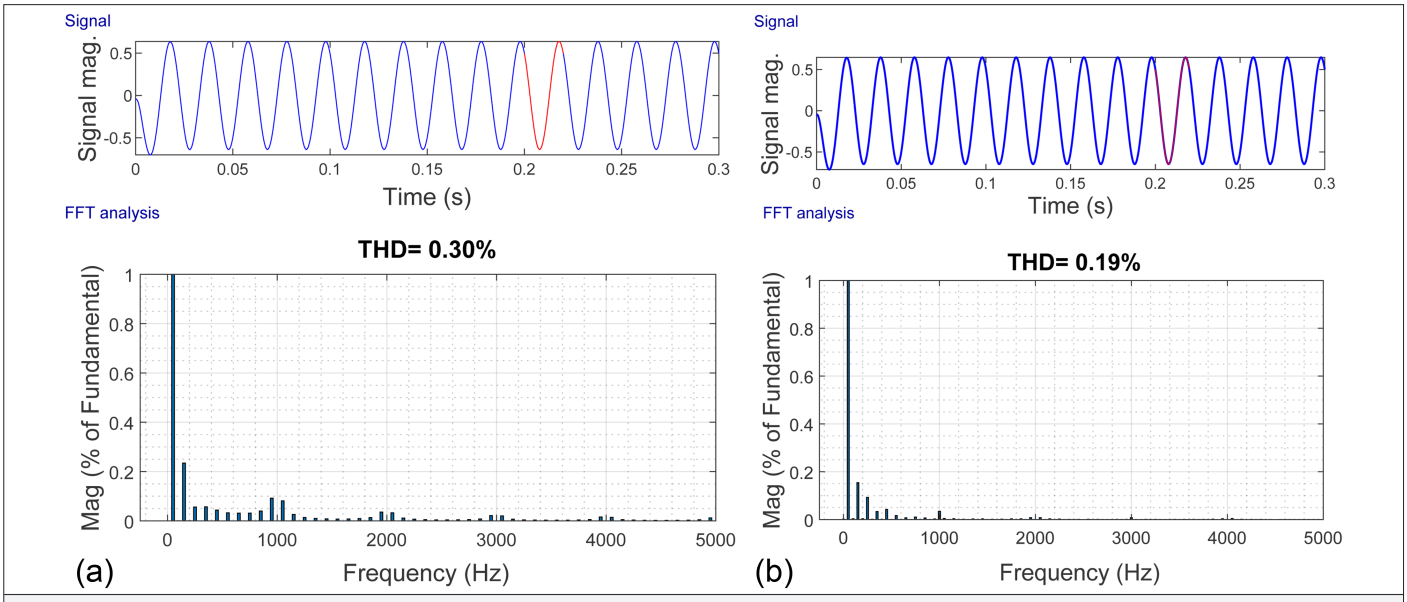


Fig. 9. Spectral analysis of the output current of the second filter with (a) three-level and (b) five-level inverters.

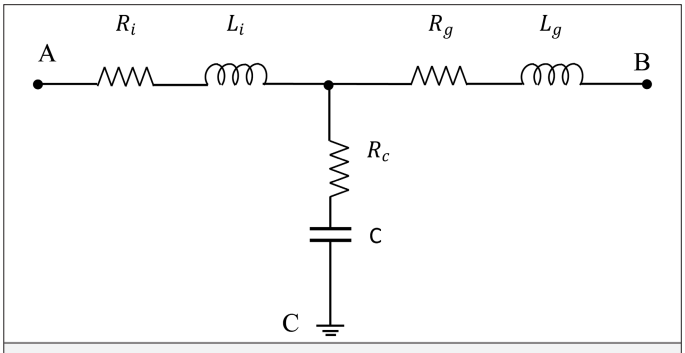


Fig. 10. Star configuration of the LCL filter.

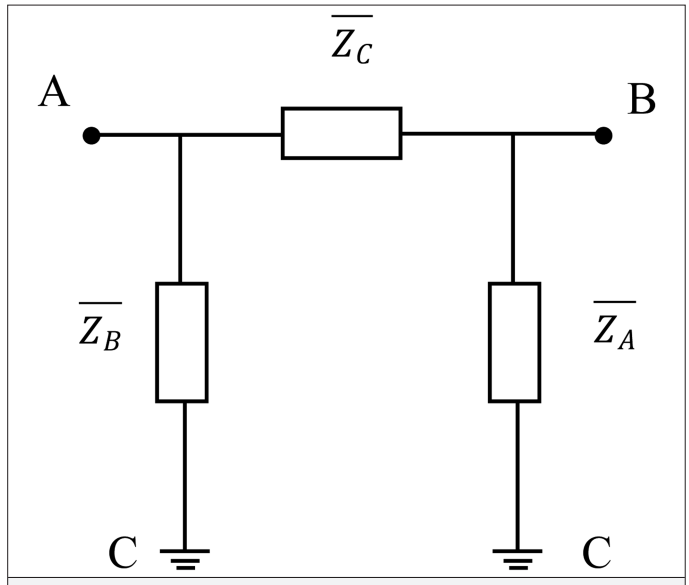


Fig. 11. Equivalent delta configuration of the LCL filter.

VII. SIMULATIONS

This section is devoted to the simulation results of the previously studied installations. Firstly, a comparative study of the three structures with the three different inverter topologies using the same filter is adopted; the first structure represents the installation with a two-level inverter while the second and the third have the same architecture as the first one except that they are connected to the three and five-level inverters, respectively. Secondly, after the critical analysis of the first study, a new simulation with two inverter topologies (three- and five-level inverters) is made after optimization of the first filter. Closing with the exploitation of the installation results in the five-level inverter with the new filter that cancels the third order harmonic. The simulation tests are performed under MATLAB/SIMULINK platform, with the parameters presented in Table II.

Fig. 8 shows simulation results of the first filter with the three inverter topologies. The spectral analysis in Fig. 8(a) shows a THD of 5.11% accentuated in the low-frequency region. This finding shows the insufficient synchronization conditions with the grid. The harmonic distortion rates in Fig. 8(b) and 8(c) show a remarkable decrease of 0.32% and 0.24%, respectively, which proves the amazing efficiency of the multi-level inverters.

Fig. 9 shows the harmonic ratio of the two installations, namely the three- and five-level inverters, with the optimized filter. It should be noted that even though the filter parameters were reduced after resizing, the THD decreased (0.30% for the three-level inverter and 0.19% for the five-level inverter) which means a reduction in the cost of the installation.

This simulation test is performed to discover the behavior of the five-level inverter installation with the third filter. The most important

TABLE II. SUMMARY OF THE THREE FILTERS' THD

	LCL1 (%)	LCL2 (%)	LCL3 (%)
2N	5.11	–	–
3N	0.32	0.30	–
5N	0.24	0.19	0.25

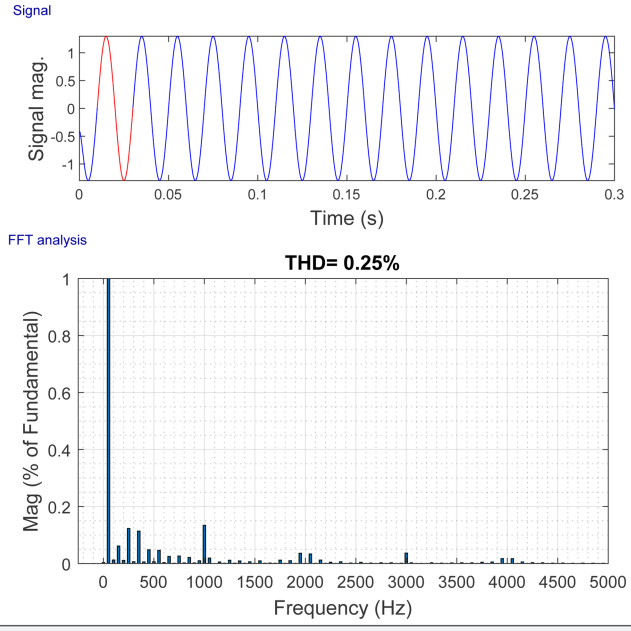


Fig. 12. Spectral analysis of the output current of the third filter with the five-level inverter.

TABLE III. PARAMETERS OF THE INSTALLATION

Active power, P	300 W
Reactive power, Q	0 VA
Grid frequency, f	50 Hz
Compound grid voltage, E_n	380 V
Simple voltage, E_{ph}	220 V
Direct voltage, V_{dc}	400 V
Switching frequency, f_{sw}	5 or 10 kHz

TABLE IV. CONTROL PARAMETERS

	Current Loop	Voltage Loop
K_p	0.87	0.37
K_i	3.39×10^{-9}	3.39×10^{-6}

observation in Fig. 12 is the reduction of the third order harmonic and optimization of the filter parameters. Moreover, the THD of the line current of the installation ensures the coupling with the grid since it presents a minimal value of 0.25%. Table I shows the parameters of the LCL1 filter with the switching frequencies 5 kHz and 10 kHz.

TABLE V. FILTER PARAMETERS WITH 10 KHZ SWITCHING FREQUENCY

	R_i (Ω)	L_i (H)	R_c (Ω)	C (μF)	R_g (Ω)	L_g (H)
LCL1	200	1.04	160.51	0.66	8	2.30×10^{-3}
LCL2	200	0.8	160.51	0.66	8	1.8×10^{-3}
LCL3	160.51	0.17	160.51	6.61	8	3.55×10^{-4}

Table III shows the harmonic distortion rates for the installations previously presented in the simulation section. From this comparative study, it appears that the five-level inverter shows the best result in the case of the THD and therefore a good waveform. The second filter LCL2 represents an improvement of the THD compared to the first filter LCL1 by minimizing the cost of the installation and by respecting the coupling conditions. Concerning the optimized filter LCL3, the harmonics of the signal are strongly reduced while ensuring the criteria of the connection to the grid and by cancelling the third order harmonic.

The parameters of the voltage and current control loops using the identification method and optimal symmetry are shown in Table IV.

The component parameters of the three LCL filters with the 10 kHz switching frequency are shown in Table V.

VIII. CONCLUSION

This paper presents performance improvement of the grid-side wind power conversion chain. Such enhancement will be provided by adopting multi-level inverter topologies, namely, the three-level NPC inverter and the five-level inverter. The use of multi-level inverters significantly improves the THD of the outputs, which offers, firstly, a gain margin concerning the filter parameters, while respecting the requirements of grid connection imposed by the Institute of Electrical and Electronics Engineers (IEEE) Recommended Practices and Requirements for Harmonic Control in Electric Power Systems. Secondly, the possibility of resizing the filter taking into account the cancellation of the third order harmonic is the most disturbing criterion.

Peer-review: Externally peer-reviewed.

Author Contributions: Concept – W.E.M.; Analysis and/or Interpretation – W.E.M., M.M.; Writing Manuscript – W.E.M.; Critical Review – S.E.D., L.L.

Acknowledgments: The authors would like to thank the anonymous reviewers for their helpful and constructive comments that have greatly contributed in improving the final version of the paper. They would also like to thank the Editors for their generous comments and support.

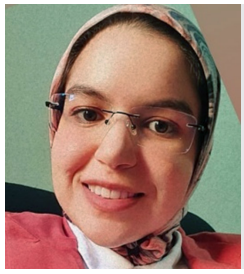
Conflict of Interest: The authors have no conflicts of interest to declare.

Financial Disclosure: The authors declared that this study has received no financial support.

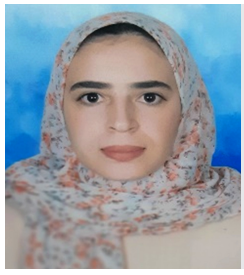
REFERENCES

1. Organisation for Economic Co-Operation and Development (OECD). *World Energy Outlook 2015*. Paris, France: OECD/International Energy Agency (IEA), 2015.

2. D. Feldman et al., *Photovoltaic System Pricing Trends: Historical, Recent, and Near-Term Projections (2015 Edition)*. CO, USA: National Renewable Energy Laboratory (NREL), 2015.
3. B. Aboagye, S. Gyamfi, E. AntwiOfosu, and S. Djordjevic, "Status of renewable energy resources for electricity supply in Ghana," *Sci. Afr.*, vol. 11, p. e00660, 2021.
4. X. Peng et al., "EALSTM-QR: Interval wind-power prediction model based on numerical weather prediction and deep learning," *Energy*, vol. 220, no. 3, p. 119692, 2020.
5. J. F. Walker and N. Jenkins, *Wind Energy Technology*. Chichester, England: John Wiley & Sons, Inc., 1997.
6. Global Wind Energy Council (GWEC). *Global Wind Reports 2021*. Brussels, Belgium: GWEC, 2021.
7. C. Li, G. Tang, X. Xue, A. Saeed, and X. Hu, "Short-Term Wind Speed Interval Prediction Based on Ensemble GRU Model," in *IEEE Transactions on Sustainable Energy*, vol. 11, no. 3, pp. 1370–1380, July 2020. [CrossRef]
8. O. Anaya-Lara, N. Jenkins, J. Ekanayake, P. Cartwright, and M. Hughes, *Wind Energy Generation Modelling and Control*. Chichester, England: John Wiley & Sons, Inc., 2011.
9. C. Hang, L. Ying, and N. Shu, "Transistor open-circuit fault diagnosis in two-level three-phase inverter based on similarity measurement," *Microelectron. Reliab.*, vol. 91, no. 2, pp. 291–297, 2018.
10. S. El Daoudi, L. Lazrak, and M. A. Lafkih, "Sliding mode approach applied to sensorless direct torque control of cage asynchronous motor via multi-level inverter," *Prot. Control Mod. Power Syst.*, vol. 5, no. 1, p. 13, 2020.
11. S. El Daoudi, L. Lazrak, N. El Ouanjli, and M. A. Lafkih, "Improved DTC-SPWM strategy of induction motor by using five-level PODPWM inverter and MRASSF estimator," *Int. J. Dyn. Control*, 2020.
12. A. Ibrahim and M. Z. Sujod, "Variable switching frequency hybrid PWM technique for switching loss reduction in a three-phase two-level voltage source inverter," *Measurement*, vol. 151, p. 107192, 2020.
13. R. Sarker, A. Dutta, and S. Debnath, "Sudipta Debnath: FPGA-based variable modulation-indexed-SPWM generator architecture for constant-output-voltage inverter applications," *Microprocess. Microsyst.*, vol. 77, 2020.
14. M. Büyük, A. Tan, M. Tümay, and K. Ç. Bayındır, "Topologies, generalized designs, passive and active damping methods of switching ripple filters for voltage source inverter: A comprehensive review," *Renew. Sustain. Energy Rev.*, vol. 62, pp. 46–69, 2016.
15. H. Cha and T.-K. Vu, "Comparative analysis of low-pass output filter for single-phase grid-connected photovoltaic inverter," in *25th Ann. Appl. Power Electron. Conf. Exposition (APEC)*, 2010, pp. 1659–1665.
16. D. Sgrò, S. A. Souza, F. L. Tofoli, R. P. S. Leão, and A. K. R. Sombra, "An integrated design approach of LCL filters based on nonlinear inductors for grid-connected inverter applications," *Electr. Power Syst. Res.*, vol. 186, p. 106389, 2020.
17. F. Sevilmiş and H. Karaca, "An advanced hybrid pre-filtering/in-loop-filtering based PLL under adverse grid conditions," *Eng. Sci. Technol. An Int. J.*, vol. 24, no. 5, pp. 1144–1152, 2021.
18. E. M. Adžic, M. S. Adžic, and V. A. Katic, "Improved PLL for power generation systems operating under real grid conditions," *Electronics*, vol. 15, no. 2, pp. 5–12, 2011.
19. Y. Yang, "Direct instantaneous power control for three-level grid-connected inverters," *Int. J. Electr. Comput. Eng. (IJECE)*, vol. 6, no. 3, pp. 1260–1273, 2016.
20. N. Daou and F. Khatounian, "A combined phase-locked loop technique for grid synchronization of power converters under highly distorted grid conditions," in *IEEE Int. Multidiscip. Conf. Eng. Tech. (IMCET)*, 2016, pp. 108–114.
21. C. Gurrola-Corral, J. Segundo, M. Esparza, and R. Cruz, "Optimal LCL-filter design method for grid-connected renewable energy sources," *Int. J. Electr. Power Energy Syst.*, vol. 120, no. 5, p. 105998, 2020.
22. M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1282–1291, 2005.
23. J. L. Monroy-Morales, D. Campos-Gaona, M. Hernández-Ángeles, R. Peña-Alzola, and J. L. Guardado-Zavala, "An active power filter based on a three-level inverter and 3D-SVPWM for selective harmonic and reactive compensation, energies," *Energies*, vol. 10, no. 3, p. 297, 2017.
24. B. Malakondareddy, S. Senthil Kumar, N. Ammasai Gounden, and I. Anand, "An adaptive PI control scheme to balance the neutral-point voltage in a solar PV fed grid connected neutral point clamped inverter," *Electr. Power Energy Syst.*, vol. 110, pp. 318–331, 2019.



Wijdane El Maataoui received her Electrical Engineering degree from Higher Normal School for Technical Education, Mohammedia, Morocco, in 2020. She is currently pursuing a Doctorate degree in Sultan Moulay Slimane University, Faculty of Science and Technology, Beni-Mellal, Morocco. Her research interests are in control of renewable energy systems and electric machines.



Soukaina El Daoudi received her B.S. degree in Electronics and Industrial Systems from Sultan Moulay Slimane University, Beni-Mellal Morocco, in 2014, and an M.S. degree in Automatic, Signals and Systems from Sidi Mohamed Ben Abdellah University, Fes, Morocco, in 2016. She is currently pursuing a Doctorate degree in Sultan Moulay Slimane University, Faculty of Science and Technology, Beni-Mellal, Morocco. Her research interests are in power electronics, electrical motors, and their digital controls.

Loubna Lazrak received her Electrical Engineering degree in 1993, and the Advanced Higher Studies Diploma (D.E.S.A) in 2002 from the National Superior School of Electricity and Mechanics (ENSEM), Casablanca, Morocco. She is currently a professor of electric machines and construction in the Electrical Engineering Department, Sultan Moulay Slimane University, Faculty of Science and Technology Beni-Mellal, Morocco. Her research interests are in control of renewable energy systems and electric machines.

Mustapha Mabrouki currently works at the Physics Department (Full Professor), Sultan Moulay Slimane University, Faculty of Science and Technology, Beni-Mellal, Morocco. His research interests are in smart grid and smart cities (optimization models for balancing energy), photovoltaic materials synthesis and integration, phosphates and derivatives, biotechnology, and microbiology. His current projects are 1) PROPREMA, to build photovoltaic yield maps of grid-connected mono, poly, and amorphous PV modules for all of Morocco with land calibration on 20 identical plants; 2) AFM project; 3) Phosphate project; 4) Solar Decathlon Africa 2019 competition.