

# Rail-to-Rail Buffer Amplifier with Adaptive Biasing for Flat Panel Displays

Uğur Çini<sup>ID</sup>

Department of Electrical and Electronics Engineering, Üsküdar University Faculty of Engineering, İstanbul, Turkey

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## ABSTRACT

Flat panel displays require buffers for column driving circuits. These buffers have unity gain and usually drive large capacitive loads. To maintain the rail-to-rail swing operation, most of the buffer circuits employ complementary differential pair input stage. Whenever the input voltage is close to supply voltages, one of the driving paths enters the cut-off state. In this paper, a novel adaptive biasing technique for biasing differential input pair transistors is proposed in order to maintain high driving capacity for the whole input range. In the proposed scheme, whenever an NMOS input stage enters the cut-off stage, the biasing current is boosted for the PMOS input stage and vice versa. As a result, without increasing the biasing current, driving capability of the circuit is boosted in the ranges which are close to the supply voltages. With the proposed biasing scheme, the circuit consumes 45% less biasing current with 16% better settling time as compared to the non-adaptive biased circuit. The proposed biasing circuit and liquid-crystal displays (LCD) buffer is designed using 0.35  $\mu\text{m}$  AMS technology and the SPICE results are reported. The circuit provides high slew-rate and good settling time characteristics which is comparable to the state-of-art LCD driving circuits.

**Index Terms**—Flat panel displays, rail-to-rail buffer, adaptive biasing.

## Corresponding Author:

Uğur Çini

## E-mail:

ugur.cini@uskudar.edu.tr

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## I. INTRODUCTION

High quality liquid-crystal displays (LCDs) are important design elements in consumer electronics market. Improving performance characteristics of LCD column drivers are crucial in high quality display technologies. In today's portable design market, low-power consumption is also the most important design constraint. In the design of LCD driver circuits, LCD column drivers have special importance. Especially, output buffer amplifiers of the column drivers play a key role in speed, quality, and power consumption of an LCD driver circuit. Since hundreds of buffer circuits are needed for an LCD or any type of flat panel display, low quiescent current and low power circuit structure with a smaller area is desirable. Due to the nature of the operation, usually large voltage swing is required for the LCD buffer circuits.

There are various designs proposed for the buffer amplifiers [1–5] of LCD displays. Most of them have class AB and class B working characteristics. They usually employ PMOS and NMOS differential input stages together in order to achieve rail-to-rail characteristics. In today's consumer electronics market, high slew-rate, fast response, low-power, and low-offset voltage are design constraints of the design of buffer circuits for the flat panel displays. In order to increase slew-rate and settling time, there are methods such as slew-rate enhancement circuits [4], current comparators at the output [6,7], etc. Especially, low quiescent current is desirable in today's world due to low power consumption requirements. The reason is that; a great portion of power consumption is due to the power requirement of the LCD display on a mobile phone or tablet computer.

In this paper, a novel adaptive biasing technique is proposed for the LCD buffer circuit. The proposed biasing scheme improves settling time whereas the quiescent current of the whole circuit is greatly reduced. The biasing circuit has two sensing paths for the rail-to-rail input. As the input voltage is close to negative supply, the NMOS differential pair enters the cut-off region. NMOS sensing path senses the cut-off condition and boosts PMOS differential pair

biasing current. Whenever the input voltage is close to positive supply, PMOS differential pair enters the cut-off region, then by using the PMOS sensing path, NMOS differential pair bias is boosted. As a result, high driving capability is maintained in the whole operating region which provides better settling time characteristics. Moreover, using bias current in better utilization provides lower power as well. The biasing circuit is applied to a novel class AB buffer circuit. The next section explains the operation of the buffer circuit and biasing circuit. In section III, the working characteristics are analyzed and the circuit is compared to previous works. Section IV summarizes the results.

## II. BUFFER AND BIASING SCHEME

A simplified diagram of the proposed buffer circuit is shown in Fig. 1. The structure is based on two complementary current mirror-based Operational Transconductance Amplifiers (OTAs) at the input stage together with pre-biased output stage. The output is driven using  $M_{OP}$  and  $M_{ON}$  output transistors. As a result, two-stage amplifier stage with unity gain feedback is employed. One of the OTAs with transconductance  $g_{mp}$  has PMOS differential pair input stage, and the other one with transconductance  $g_{mn}$  has NMOS differential pair. The adaptive biasing scheme is not included in Fig. 1 and will be explained in detail in the following paragraphs. The input stage is based on two current mirror OTAs which have large input common mode range compared to active loaded differential pairs, so that, through most of the input swing range, both of the OTAs is active in the operation. The output bias circuit which is shown inside dotted lines in Fig. 1 keeps each of the output transistors close to active region in the extreme common mode input levels. It should be noted that only a small portion of the bias current is supplied for the output biasing in order to keep the output transistors within the pre-biasing condition.

The circuit works even when the output biasing is not available, however, when one of the inputs of the output drivers are in the cut-off stage, the related output transistor input is not

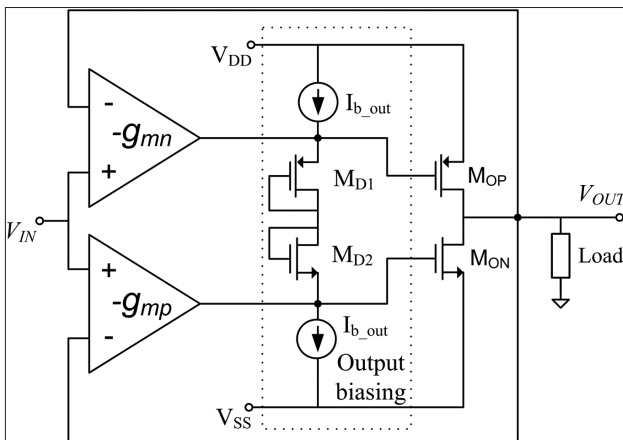


Fig. 1. Simplified schematics of the voltage buffer.

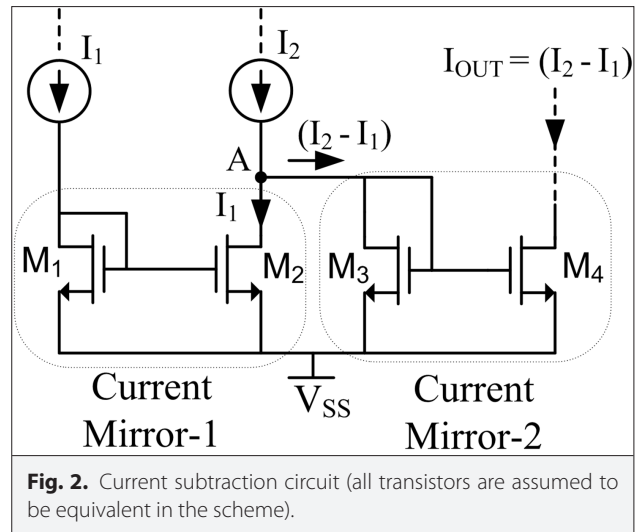


Fig. 2. Current subtraction circuit (all transistors are assumed to be equivalent in the scheme).

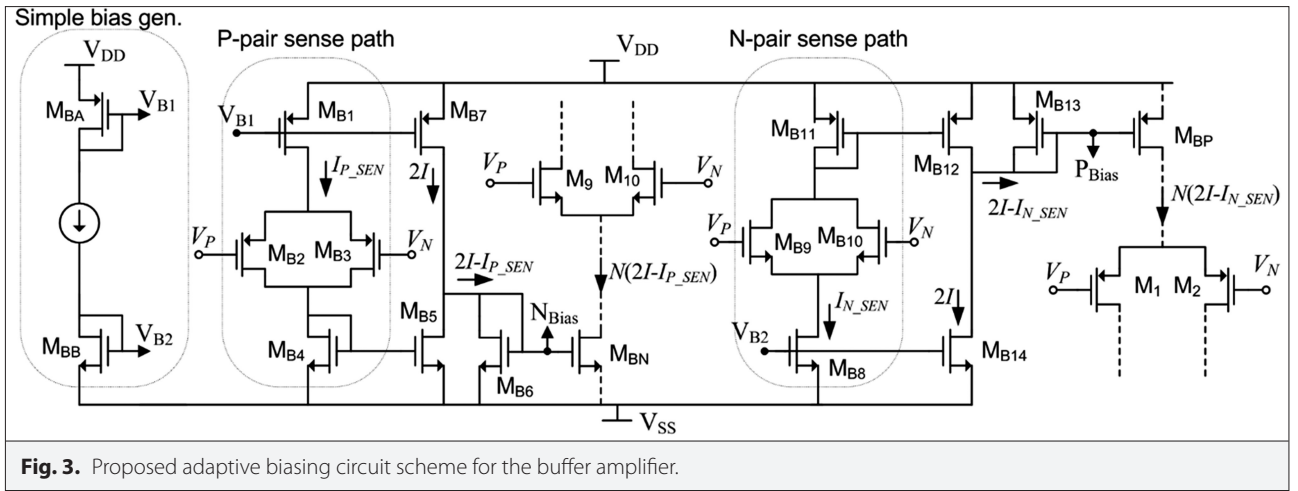
properly biased; then excessive output current is driven as one of the output transistors which would have a floating input. In order to prevent extreme power consumption, output biasing plays an important role in the circuit structure.

The adaptive biasing technique is based on sensing the differential pair circuits' cut-off points by two sensing circuits both for PMOS and NMOS biasing, and then, current subtraction circuit is used to adjust the required bias current both for PMOS and NMOS differential pairs. Due to adaptive biasing, a current saving at about 50% can be achieved.

The current subtraction circuit is realized by merging two current mirrors as shown in Fig. 2. Assuming all the transistors have same size, as current  $I_1$  is applied to the first current mirror, the current  $I_1$  is copied to transistor  $M_2$ . Another current  $I_2$  is applied to node A in the circuit. As a result, current  $(I_2 - I_1)$  flows from drain to source of  $M_3$ , due to Kirchoff's current law. As a result,  $(I_2 - I_1)$  current is copied by Current Mirror 2. Here, it is assumed that  $I_2 > I_1$ , and channel length modulation and other non-idealities are neglected. If the sizing of each transistor is not equivalent, then the current subtraction circuit equation is:

$$I_{OUT} = \left[ I_2 - \left( \frac{W}{L} \right)_2 I_1 \right] \left( \frac{W}{L} \right)_4 \left( \frac{W}{L} \right)_3 \quad (1)$$

where  $W$  and  $L$  are width and length of the related transistors [8]. Here, the channel length modulation and other non-ideal conditions are neglected, and  $I_1$  and  $I_2$  represent the input currents as shown in Fig. 2. In the adaptive biasing scheme, selection of output transistor (which is  $M_4$  in Fig. 2) having larger width ( $W$ ) would be a better choice, since sensing circuit should consume much less power than the output current.



**Fig. 3.** Proposed adaptive biasing circuit scheme for the buffer amplifier.

Adaptive biasing circuit based on current subtraction technique is depicted in Fig. 3. The adaptive biasing circuit has two sensing paths as p-pair sensing and n-pair sensing which detects cut-off conditions for PMOS differential pair and NMOS differential pair, respectively.  $I_{p\_SEN}$  and  $I_{n\_SEN}$  are the sense path currents for the p-pair sensing and n-pair sensing, respectively, both of which are assumed to be equal to current  $I$ . The dashed lines are not the part of the biasing circuit; they are differential input stages of the buffer circuit. In this scheme, it is assumed that  $I_{p\_SEN} = I$ . Whenever both PMOS and NMOS input stages are active, the current flowing into drain to source of  $M_{B6}$  is  $(2I - I_{p\_SEN}) = I$ . The subtracting is handled by current subtraction circuit which is realized by  $M_{B4}$ - $M_{B6}$  transistors. If the sizing ( $W/L$ ) of the  $M_{BN}$  is  $N$  times larger than sizing of  $M_{B6}$ , drain current of input stage is  $N$  times  $I$ . If the input voltage applied to the buffer is close to positive supply voltage, that is,  $V_{DD}$ , the PMOS differential input stage enters the cut-off region, so that the current source of the differential pair also enters. The p-pair sense path emulates this condition. As a result,  $I_{p\_SEN}$  current cannot flow through the sense path, in this condition  $I_{p\_SEN}$  is zero, so that  $2I$  current flows into the drain to source of  $M_{B6}$  transistor in Fig. 3.

The same applies to the N-pair sense path, where  $I_{n\_SEN} = I$ . As a result, whenever both NMOS and PMOS differential pairs are active, the bias currents of each path are  $N^*I$ . If NMOS input stage enters the cut-off region, PMOS bias current becomes  $2N^*I$ . If PMOS input stage enters cut-off region, NMOS bias current becomes  $2N^*I$ . As a result, total bias current for the input stages are kept as  $2N^*I$ .

The whole buffer circuit diagram is shown in Fig. 4, where the bias generator is also depicted in Fig. 3.  $N_{Bias}$  and  $P_{Bias}$  are the bias voltages which are generated by the proposed bias generator circuit shown in Fig. 3. The buffer circuit shown in Fig. 4 consists of mirrored OTA type first stage by two differential input pairs, and output stage with transistors  $M_{ON}$  and  $M_{OP}$ . In the circuit, the output biasing is also provided using transistors  $M_{B01}$ - $M_{B04}$ . Whenever any of the complementary OTAs become inactive, output biasing circuit still provides biasing for

both of the output transistors  $M_{OP}$  and  $M_{ON}$  in order to maintain class AB operation properly.

The output impedance of the whole buffer can be approximated as:

$$r_{out} = \frac{r_{oOP} \parallel r_{oON}}{g_{m1}(r_{o8} \parallel r_{o5}) \parallel (r_{oB04} \parallel r_{oB01})g_{mOP}(r_{oOP} \parallel r_{oOP}) + g_{m9}(r_{o13} \parallel r_{o16}) \parallel (r_{oB04} \parallel r_{oB01})g_{mON}(r_{oOP} \parallel r_{oOP})} \quad (2)$$

$$= \frac{1}{g_{m1}g_{mOP}(r_{o8} \parallel r_{o5}) \parallel (r_{oB04} \parallel r_{oB01}) + g_{m9}g_{mON}(r_{o13} \parallel r_{o16}) \parallel (r_{oB04} \parallel r_{oB01})}$$

where,  $g_m$  is the transconductance of the related transistors and  $r_o$  is the output impedance of the related transistor.

The current source transistor of the buffer circuit  $M_{BP}$  is biased with  $P_{Bias}$  voltage whereas  $M_{BN}$  is biased with  $N_{Bias}$ , both of which are generated by the adaptive bias generation scheme which is also depicted in Fig 3.

Sizing of the remaining transistors is not critical as long as matched transistors are selected in equal dimensions. The sizing of the transistors for the proposed circuit is shown in Table I. Output biasing currents are a small fraction of OTA bias currents as  $M_{B01}$  and  $M_{B04}$  where aspect ratio ( $W/L$ ) is much smaller than  $M_{BN}$  and  $M_{BP}$  respectively.

### III. SIMULATION RESULTS AND DISCUSSION

The dynamic biasing current simulation results are shown in Fig. 5. Here, a rail-to-rail input signal is applied to the buffer circuit. Here,  $V_{DD}$  is 3V and  $V_{SS}$  is 0V. As the input swing travels through full swing, the bias current of PMOS and NMOS differential biasing currents dynamically change. In the mid supply, both of the current levels are 600 nA. Whenever  $V_{IN}$  is approaching  $V_{DD}$  level, NMOS path current which is denoted by  $N_{Diff}$  ( $I_{NDiff}$ ) in Fig. 5 is boosted and its value approaches 1  $\mu A$ . In the opposite condition, PMOS path current which is denoted by  $P_{Diff}$  ( $I_{PDiff}$ ) approaches to 1  $\mu A$ .

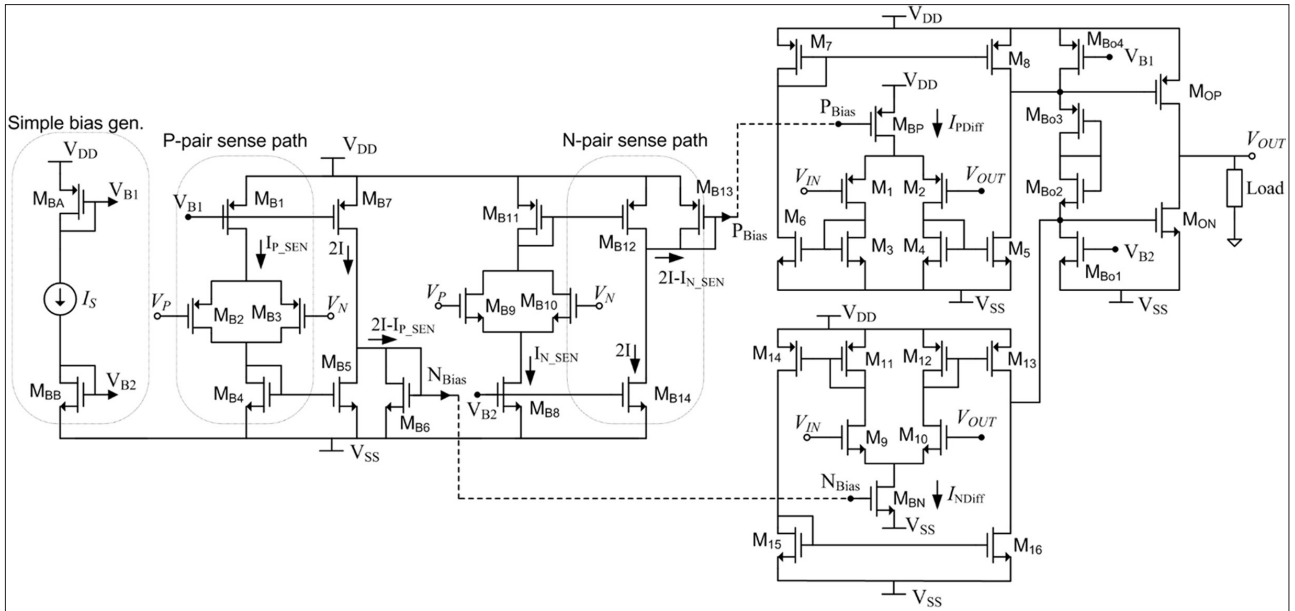


Fig. 4. Circuit schematic of the rail-to-rail buffer amplifier.

Full swing square wave input is applied to the circuit where the output load is 1000 pF. It should be noted here that a 200 Ω serial resistor is connected serially to the capacitive load, which improves stability greatly. A rail-to-rail square wave input is applied to the input of the proposed circuit and the output voltage is plotted together with the input voltage, which is shown in Fig. 6. Also, process, voltage, temperature (PVT) analysis is applied to the circuit for 5% supply voltage variation and temperature variation from 0°C to 70°C. The result plot is shown in Fig. 7, where all results reside within 5% tolerance. The circuit

is also simulated without adaptive bias circuit, i.e., simple biasing is applied to the bias input points to the proposed buffer circuit. Simulation results of the buffer circuit with and without adaptive biasing are shown in Table II. For better comparison, a figure of merit calculation is given as:

TABLE I. TRANSISTOR SIZING OF THE PROPOSED CIRCUIT

Transistor	Dimensions (W/L) (μm/μm)
$M_{BA}, M_{BB}$	30/1
$M_{B1}, M_{B2}$	5/1
$M_{B7}, M_{B14}$	10/1
$M_{B4}-M_{B6}, M_{B11}-M_{B13}$	7.5/1
$M_{B2}, M_{B3}, M_{B9}, M_{B10}$	2/0.5
$M_1, M_2, M_9, M_{10}$	2/0.5
$M_3-M_9, M_{11}-M_{16}$	10/1
$M_{B1}, M_{B4}, M_{BN}, M_{BP}$	30/1
$M_{Bo1}, M_{Bo4}$	5/1
$M_{Bo2}, M_{Bo3}$	0.5/3
$M_{OP}$	45/0.35
$M_{ON}$	15/0.35

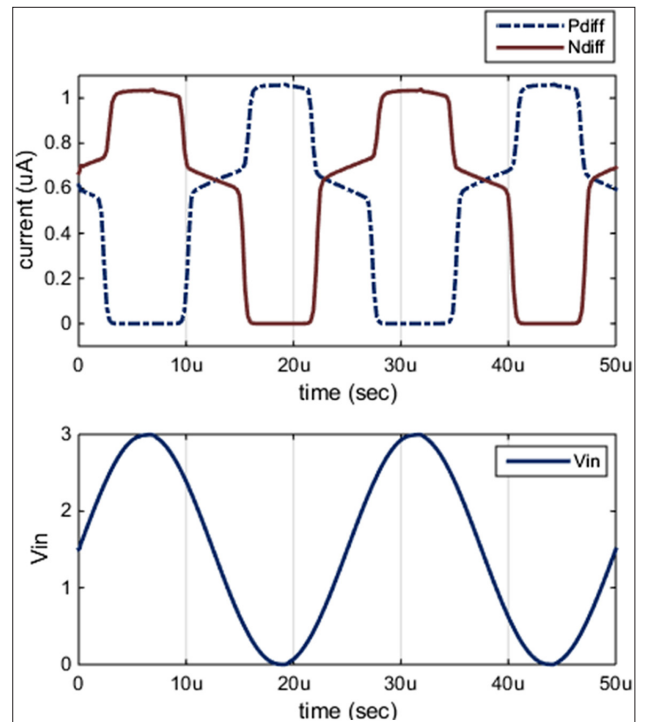
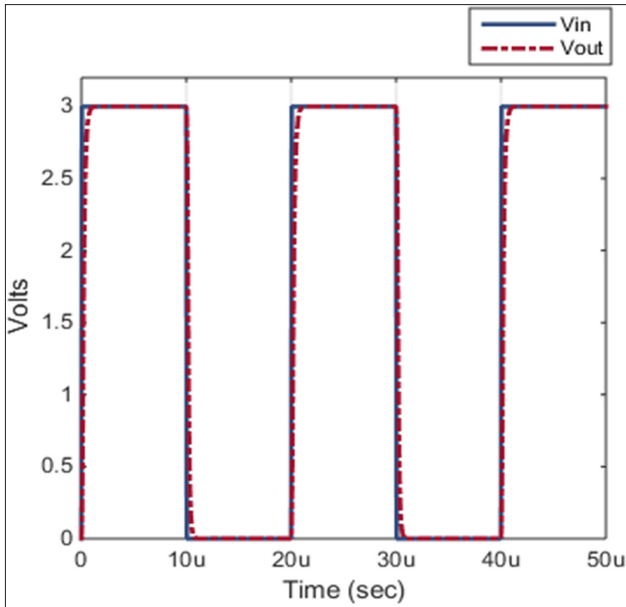


Fig. 5. PMOS and NMOS differential bias current variation with rail-to-rail input voltage. As input reaches to supply voltage, one of the bias supply currents Ndif (Pdif) is boosted.

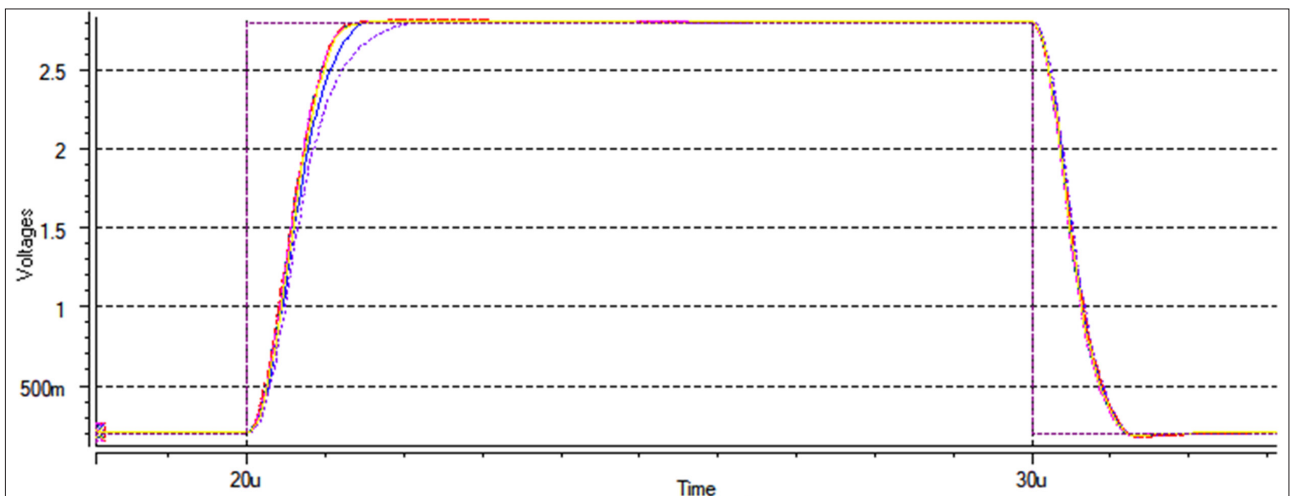


**Fig. 6.**  $V_{in}$  and  $V_{out}$  plots for 0–3 V square wave input with 1 nF load at the output.

$$FOM = \frac{C_L}{T_{Settling} \cdot I_Q} \quad (3)$$

where,  $C_L$  is the load capacitance (pF),  $T_{Settling}$  is the settling time of the circuit ( $\mu$ s), and  $I_Q$  is the quiescent current of the circuit ( $\mu$ A).

It is clear that the proposed adaptive biasing scheme provides great advantage. The bandwidth of the circuit seems lower due to lower quiescent current, however, settling time and slew rate are the critical parameters of the circuit and high voltage response performance is crucial due to the nature of the circuit.



**Fig. 7.** Large signal input response for the process, voltage, temperature (PVT) corners.

**TABLE II.** PERFORMANCE PARAMETERS OF THE CIRCUIT

Parameter	Buffer Without Adaptive Bias	Buffer With Adaptive Bias
Supply voltage (V)	3	3
Quiescent current ( $\mu$ A)	4.5	1.9
Settling time ( $\mu$ s)	1.6	1.35
Pos./neg. slew rate (V/ $\mu$ s)	3.3/3.5	3.2/3.4
In/out range (% $V_{DD}$ )	100	100
Unity gain bandwidth (kHz)	2 MHz	600 kHz
Load capacitor (pF)	1000	1000
FOM	138.9	389.9

A 10 kHz 1.5 V amplitude sinusoidal input is applied to the input to measure the total harmonic distortion (THD). SPICE report for the THD is 0.76%, which shows the circuit provides excellent buffering capability for the large AC signals as well.

A small signal input is also applied to show the small signal performance characteristics. A 100 mV signal is applied to the input and the result is shown in Fig. 8. A very small overshoot is recorded in the small signal square wave input, which is quite satisfactory for the buffer circuit. Frequency response plot is also shown in Fig. 9 together with phase response of the circuit in closed loop mode which shows the stability of the circuit as well.

The proposed buffer circuit is also compared with previous design techniques as shown in Table III [2,6,9-13]. The results of the simulations are quite satisfactory. The work in [11] has closer results with the proposed scheme. However, [11] has three-stage amplifier where the middle stage consists of a

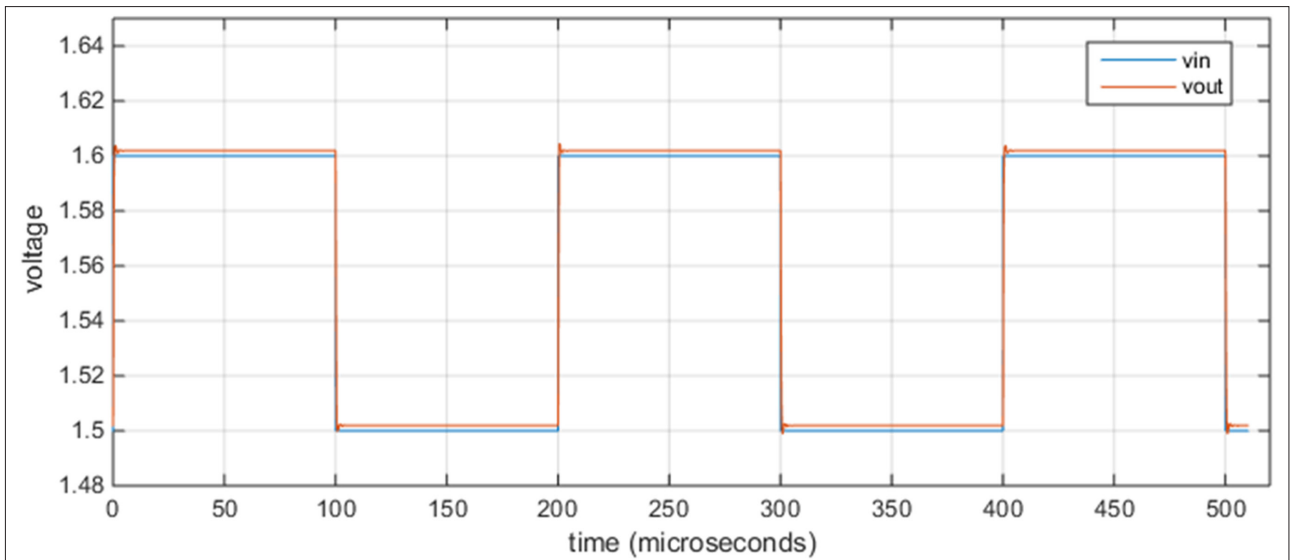


Fig. 8. Small signal response of the amplifier for a 5 kHz small signal input voltage.

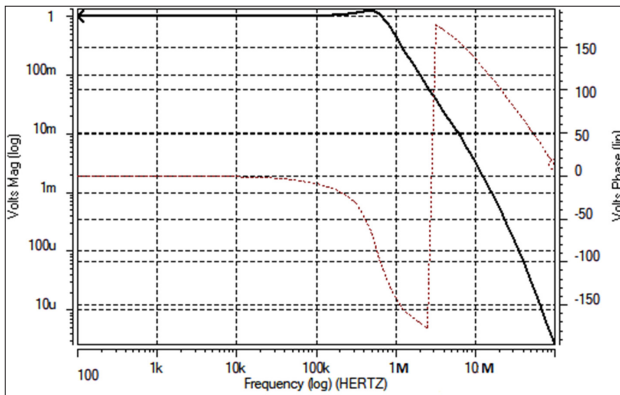


Fig. 9. Frequency response of the amplifier.

simple inverter circuit that may cause excessive power consumption in switching. Design in [13] exhibits slightly better FOM value. However, it requires bulk biasing and special layout techniques with isolated bulk islands in the layout which increases area, requires more complex layout techniques.

#### IV. CONCLUSIONS

In this paper, a power efficient rail-to-rail buffer circuit with adaptive biasing technique is proposed where it provides lower quiescent currents. The proposed biasing scheme in the buffer circuit greatly economizes the power, and provides better settling time results when compared to non-adaptive biasing scheme. The circuit requires only 1.9  $\mu\text{A}$  biasing current with 5.7  $\mu\text{W}$  biasing power requirement for

TABLE III. PERFORMANCE COMPARISON OF VARIOUS FLAT PANEL BUFFER AMPLIFIERS

	[2]	[6]	[9]	[10]	[11]	[12]	[13]	Proposed (Adaptive Biasing)
Operation class	B	B	AB	B	B	AB	AB	AB
CMOS technology ( $\mu\text{m}$ )	0.8	0.6	0.6	0.35	0.35	0.6	0.35	0.35
Supply voltage (V)	5	3	5	3.3	3.3	5	3	3
Quiescent current ( $\mu\text{A}$ )	24	3.5	30	7.4	1.6	32	1.63	1.9
Load capacitor (pF)	600	1000	680	600	1000	1000	1000	1000
Settling time ( $\mu\text{s}$ )	5.5	1.7	1.3	8	1.45	0.71	1.11	1.1
In/out range (V)	1/5	0/3	0.15/4	0.05/3.25	0/3.3	0/3	0/3	0/3
In/out range (% $V_{\text{DD}}$ )	80%	100%	77%	97%	100%	100%	100%	100%
FOM (pF/ $\mu\text{s}\cdot\mu\text{A}$ )	4.5	168.1	17.4	10.1	431.0	44.0	552.7	389.9

each buffer circuit in the quiescent conditions. The results are comparable with the state of the art flat-panel buffer driver circuits. Future study includes applying the proposed adaptive bias to the other LCD buffer circuits. Fabrication of the proposed circuit is also kept for future work. The proposed adaptive biasing technique can also be applied to various types of rail-to-rail circuit applications such as operational amplifier and operational transconductance (OTA) circuits, current-mode circuits such as current conveyors and various buffer applications.

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Uğur Çini received B.Sc. degree in Electronics Engg. from Yıldız Tech. Univ. Then, he received degrees of M.Sc. (2003) & Ph.D. (2010) in Electrical Engg. from Bogazici Univ. He has worked in ISBAK Inc. as R&D engineer (2008-2013). Currently, he is an assistant professor at Uskudar University. His research interests are VLSI design, computer arithmetic and embedded systems.